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FINAL REPORT

R. F. TEST CONSOLE

Contract No. 950144

This work was performed for the Jet Propulsion Laboratory,  
California Institute of Technology, sponsored by the  
National Aeronautics and Space Administration under  
Contract NAS7-100.

Date: 10 April 1965

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## I. Introduction

The Radio Frequency Test Console is a precision transmitter-receiver system. The system input is a complex baseband spectrum. The transmitter subsystem yields a 50 mc carrier, angle modulated (PM or FM) as a function of the modulation spectrum. The transmitter output is linearly summed with band limited gaussian noise. The noise power density and noise bandwidth of the noise source is calibrated. The linear signal to noise summer exhibits 100 DB dynamic range of signal to noise ratios in 0.1 DB increments. The receiver subsystem is comprised of a phase lock PM receiver, phase lock FM receiver and conventional FM receiver. Further, the transmitter includes an amplitude modulator and the PM receiver a coherent amplitude demodulator. The system simulates the spacecraft and DSIF transmitting and receiving subsystems for the purpose of accurately testing developmental modulation, coding and synchronization techniques for application to future telemetry, command, video and ranging systems.

### A. Program Goals

The Phase I program goals are outlined in the Statement of Work and JPL Spec. GPG-15062-DSN. Briefly, the phase I effort was organized as both a study program and a design and fabrication effort. The design program included the design, fabrication and test of the Linear Signal to Noise Summer. The study portion of phase I included a design study of the P.M. Transmitter, P.M. Receiver, Phase Noise Instrumentation, F.M. Transmitter, F.M. Receiver Test Plan and Test Instrumentation. The output of each study includes both a design plan and unit specifications for the Phase II design and fabrication program.

FOREWORD

The enclosed report is a summary of the study work and Linear Signal/Noise Summer development completed for the Jet Propulsion Laboratory on contract number 950144. This report covers the work performed in the period from March 1964 through March 1965. The objective of the phase 1 program was to prepare the design plan for the FM/AM Sub-System, the FM/AM Sub-System and to design and fabricate the Linear Signal to Noise Summer. The work has been completed and the results achieved on the Linear Signal to Noise Summer meet the rigid performance goals established at the start of the program. Each portion of this work is documented in appendices A through K. These reports form a part of this final report but are submitted as separate documents.

The following individuals were the principal contributors to this program:

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## B. SUMMARY AND CONCLUSIONS

The design and development of the Linear Signal to Noise Summer in the phase 1 program [resulted in a system of equipment which met or exceeded the rigid performance goals] established at the start of the program. [The principal design parameters, design goals, and test results] are listed below.

<u>Parameters</u>	<u>Performance Goals</u>	<u>Test Results</u>
S/N Dynamic Range	0 to 100 DB	0 to 100 DB
Absolute Accuracy	$\pm 0.3$ DB over 4 hour period	40 samples from 250,000 population, 95% confidence that 95% of all settings within $\pm 0.155$ DB
Signal Power Stability	$\pm 0.1$ DB over 4 hour period	
Noise Power Stability	$\pm 0.1$ DB over 4 hour period	
S/N Ratio Stability		$\pm 0.013$ DB 4 hour period includes both signal and noise power stability
Spectral Density	Constant within $\pm 0.05$ DB From 48 to 52 Mcs.	less than $\pm 0.05$ DB, 48 to 52 Mc.

The original criterion outlined by JPL representatives was that work on the FM/AM and FM/AM Sub-systems would not be started until the feasibility of the Linear Signal to Noise Summer development was verified. Therefore, the design and development of these other Sub-systems may now be initiated since the feasibility of meeting this criterion has been documented.

The study portion of the Phase 1 effort included an investigation and comparison of a Locked Oscillator Phase Modulator and a Deviation Multiplication Phase Modulator. The Locked Oscillator Phase Modulator investigation



includes several loop designs. The loop design selected, exhibits a closed transfer function whose group delay is constant (linear phase) over the baseband. The required filtering, phase response and out of band rejection characteristics of the conventional Deviation Multiplication Phase Modulator are severe. The stringent specifications impose design problems on both units; however, the Locked Oscillator Phase Modulator is recommended for fabrication on the following basis:

1. Simplicity
2. Superior Phase Response
3. Adequate Spurious Rejection
4. More Applicable to a Combined PM/FM Modulator.

The design study also includes an investigation of the requirements of the PM Receiver, FM Transmitter, FM Receiver, Phase Noise Instrumentation, Test Plan and Test Instrumentation. The P. M. and F. M. Receiver investigation yielded a detailed block diagram and the dynamic range of noise and signal power levels from input to output. The linearity, noise figure, bandwidth, limit levels, oscillator stability characteristics are included.

The F. M. Transmitter study yielded a multiple loop system for the AFC mode. One loop is organized to transfer the linearity of the discriminator to the VCO within the constraints of the AFC loop parameters. The second loop (AFC loop) references the carrier frequency to the system master clock. This arrangement decreased the range of applicable modulation indices originally requested but this is required in order to meet the residual F.M. specification.

The Test Plan and Test Instrumentation Study included an investi-

gation of equipment required to correlate system performance against the system specification.]

The limited experimental effort included an investigation of precision VCO short term stability. The  $1-H(S)$  transfer function of the carrier tracking loop with  $2 B_{LO}$  of 3.0 cps was simulated. The resulting filtered phase noise of two locked oscillators was experimentally determined. The results indicated that the minimum value of  $2 B_{LO}$  must be 3.0 cps or greater to constrain the RMS phase noise to one degree.

## II. R. F. Test Console System Description

### A. SYSTEM DESCRIPTION

A functional block diagram of the RF Test Console is shown in figure 1. The principal subsystems include 1) Linear Signal/Noise Summer Subsystem 2) PM/AM Subsystem 3) FM/AM Subsystem 4) Frequency Synthesizer Subsystem and 5) Test Instrumentation Subsystem.

A brief system review follows. The Linear Signal/Noise linearly sums noise power, with accurately known noise bandwidth and noise power density, with an angle modulated carrier (either PM or FM). Further, the S/N Summer is capable of providing accurately known S/N ratios over a 100 DB dynamic range in 0.1 DB increments. Provision is also made to simultaneously amplitude and angle modulate the carrier. The noise spectrum is centered on 50 mc and the unmodulated carrier is 50 mc. The PM baseband extends from DC to 1.5 mc with a peak deviation of four radians. The FM baseband extends from 3.0 cps to 500 KC in AFC mode and DC to 500 KC in non-AFC mode. The AM baseband extends from DC to 5 KC with  $\pm 50\%$  modulation.

The PM/AM Subsystem consists of a Phase Modulator, Amplitude Modulator and Phase coherent Receiver. Further, provision is made to measure the phase noise of the receiver locked oscillator. The demodulated baseband is the principal receiver output; however, the baseband is also centered on 5 mc for predetection recording. The predetection playback (centered on 5 mc) is up converted to 50 mc and may be substituted as a receiver input.

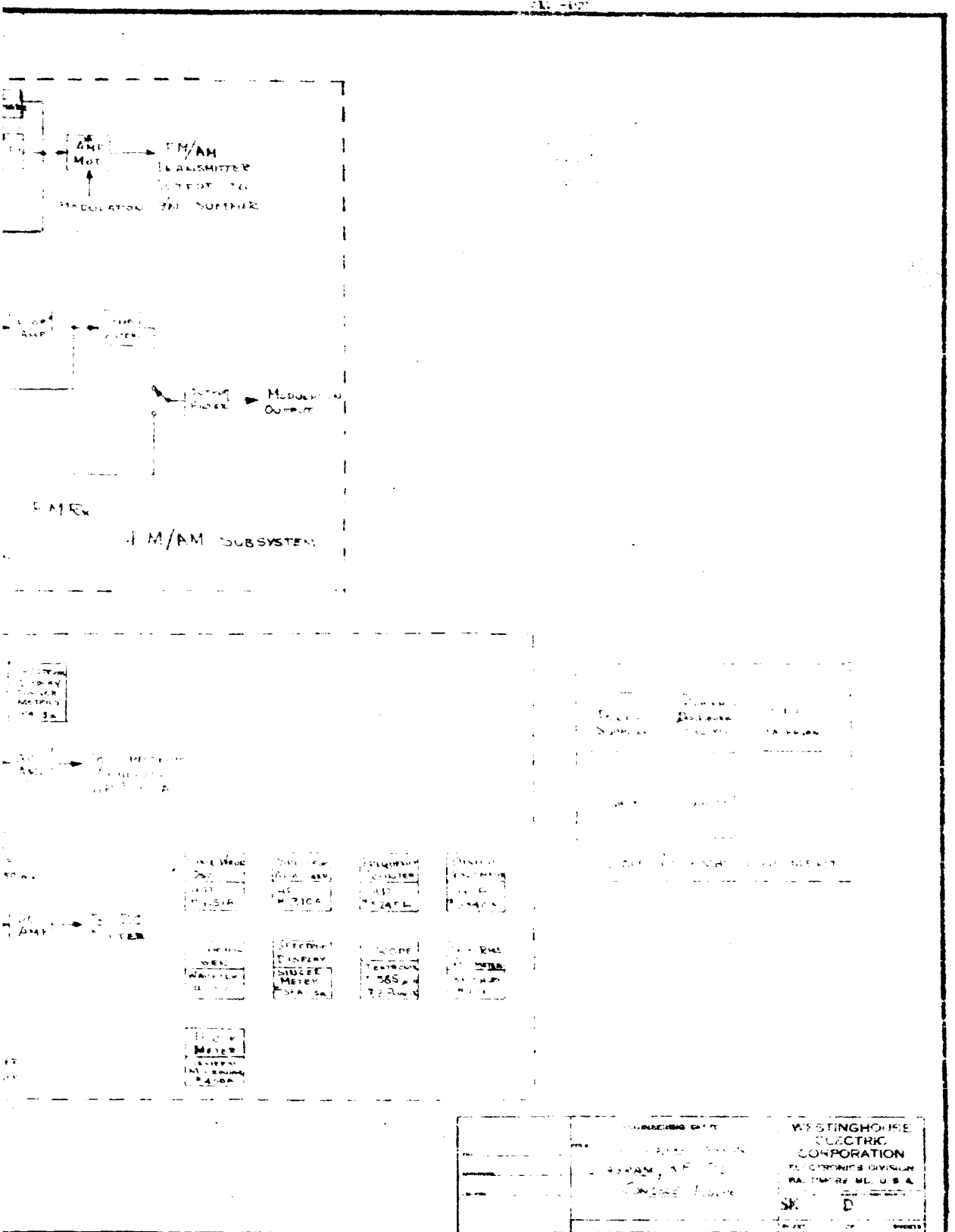
The FM/AM Subsystem consists of a Frequency Modulator that is operable either with or without AFC. A phase lock FM receiver and conventional discriminator FM receiver constitute a portion of the FM/AM Subsystem. Replaceable input and output filters are provided to test the system at various noise and information bandwidths. The frequency synthesizer provides all transmitter and test frequencies. Each frequency is coherent with a 1 mc precision standard. The amplitude modulator may be cascaded with the Frequency Modulator to provide simultaneous FM and AM. Note however, that the S/N Summer servo controls the noise power against the 50 mc modulated carrier. If the total power of the unmodulated carrier changes with modulation the resultant signal to noise ratios will be in error. Therefore, the amplitude modulator must be located between the carrier reference splitter and the signal attenuator.

The Test Instrumentation Subsystem provides a means of measuring the suppression of the angle modulated carrier. All auxiliary test equipment either purchased or fabricated is included in this subsystem.

#### B. Linear Signal/Noise Summer Subsystem

The detailed results of the Linear Signal/Noise Summer design fabrication and test appear in Appendix B of this report. The following constitutes a summary of that task. The S/N Summer specifications are listed as follows:

1. S/N Dynamic Range -----	0 to 100db
2. Absolute Accuracy -----	+ .3db over 4 hour period
3. Signal Power Stability -----	+ .1db over 4 hour period
4. Noise Power Stability -----	+ .1db over 4 hour period





5. Noise Bandwidth ----- 45 to 55 mc  $\pm$  .05 db
6. Noise Amplitude ----- Linear up to  $5\sigma$
7. Power Monitor ----- Resolution better than  
 $.05\text{db} \pm .1\text{db}$  uncertainty.

The S/N Summer block diagram is shown in Figure 2.

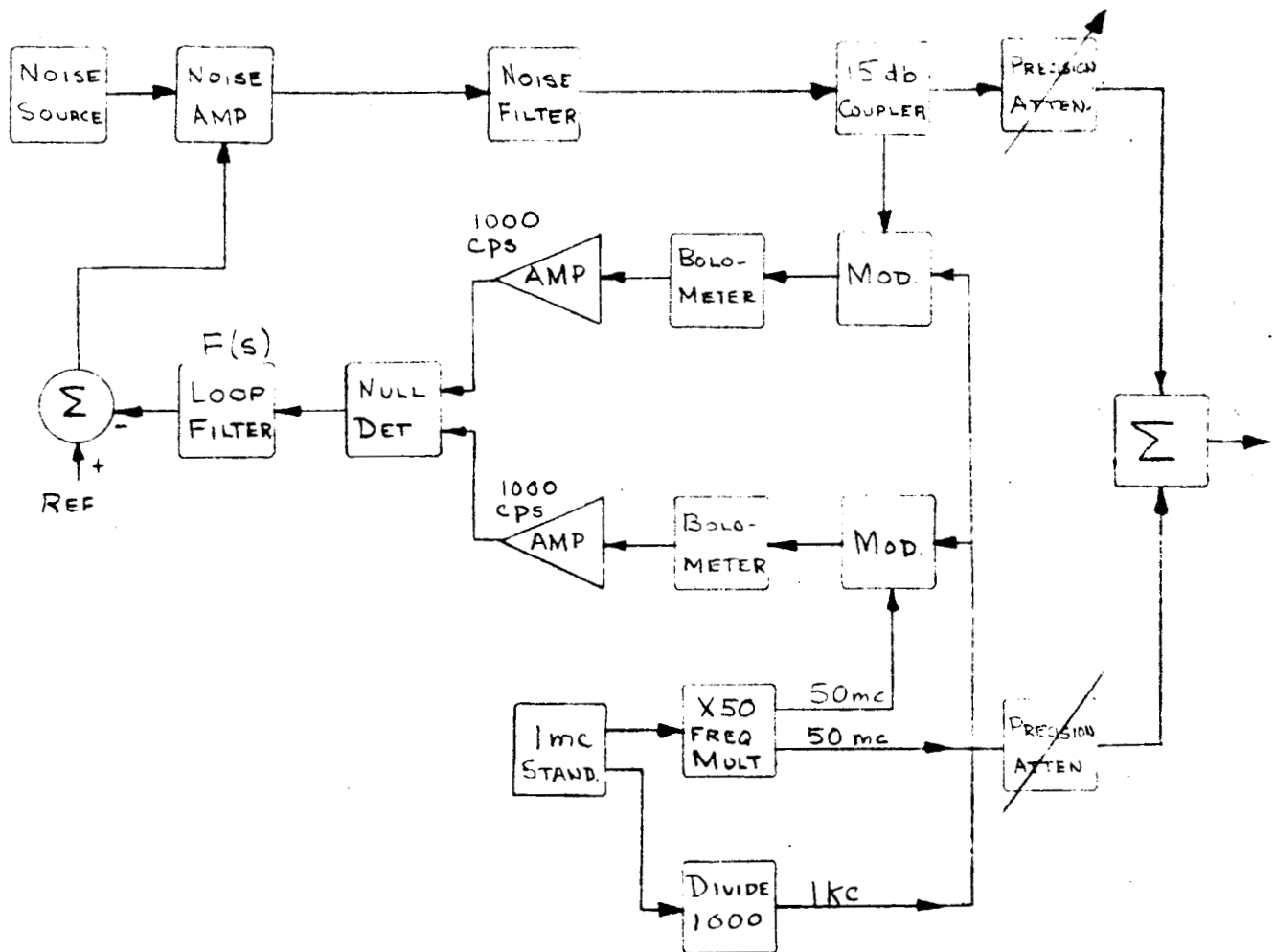


Figure 2. Simplified Block Diagram, Linear S/N Summer

The S/N Summer consists of a gaussian noise source and 50 mc carrier source. The noise source output (+ 10 db excess noise) is amplified and band limited by the noise amplifier and noise filter respectively. The band limited noise is sampled (15 db coupler) and chopped at 1 kc. The bolometer output consists of a 1 kc fundamental whose magnitude is a function of the noise power. The 50 mc carrier source is processed similarly. The resultant 1 kc tones (one a function of noise power, the other a function of carrier power) are null detected. The resultant error controls the noise power. The noise source is referenced to the signal source such that changes in the signal source are not reflected as a change in signal to noise ratio but rather as a change in absolute signal and noise power. Conversely, changes in the noise source are compensated within the constraints of the loop gain, bandwidth etc. The majority of the loop gain is contributed by the 1 kc amplifiers and is not subject to D.C. drift.

The majority of the noise power (coupler output) is linearly summed with the carrier. Precision attenuators (dynamic range 0-60 db in 0.1 db steps) are provided in both the signal and noise channels. The summer output signal to noise ratio is variable over a dynamic range of at least 100 db in 0.1 db increments. The Null Detector and 1 kc amplifiers are a modified version of the Weinschel Dual Channel Insertion loss test set. The Precision Attenuators are Weinschel model 61AS. The attenuator calibration is referenced to the Bureau of Standards.

# 1. S/N Summer Components

## a. Noise Source

The noise power density is a function of the noise source



characteristics and the passband characteristics of the noise filter and noise amplifier. The noise source vendor, Rhode & Swartz, of Munich Germany, initially measured the noise power density by a frequency translation technique. The noise density tests were made over the spectrum from 45 mc to 55 mc in 1 mc increments in a detection bandwidth of 1 kc. Further, the spectrum was tested from 50.00 to 50.01 mc in 1 kc increments in a 200 cps detection bandwidth and from 50.000 to 50.001 mc in 100 cps increments in a 6 cps bandwidth. The test set for the 6 cps increments is shown in Figure 3.

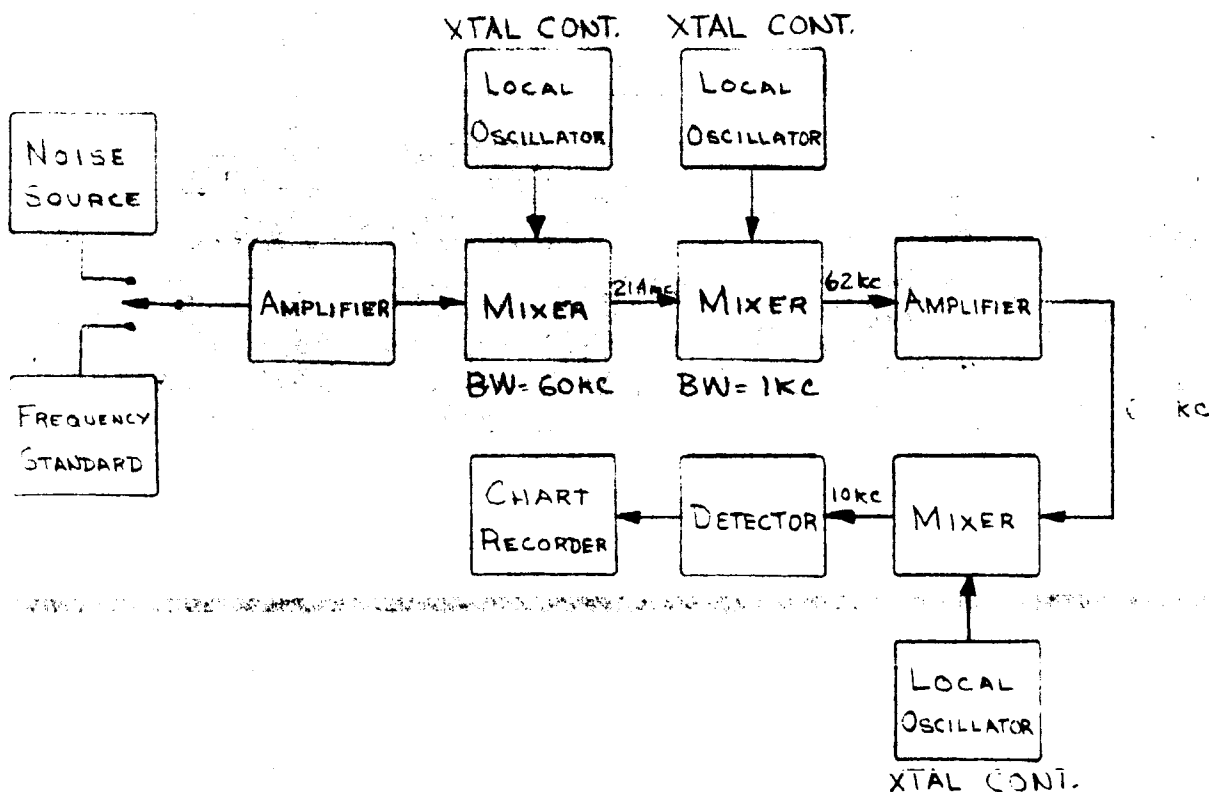


Figure 3. Spectral Density Test Set-Up

The test results are shown in Figures 4, 5, and 6.

From the results shown in Figure 6 it appears that the power density falls outside the required specification of  $\pm .05\text{db}$ . The data is inconclusive in that an insufficient amount of time was allotted to acquire a measurement at any one frequency. In this test set-up, the detected output was recorded on a strip chart. After a given period of time the chart recording was graphically integrated to get the mean value for that frequency. (The required measurement time necessary to insure 95% confidence with a  $\pm .05\text{db}$  tolerance is approximately 16 hours for each frequency at this 6 cps bandwidth.) Although it is not known exactly what time was allotted for this test it is known that the integration time was insufficient. This was not a problem at the wider bandwidths for more points could be sampled in a shorter period of time. Therefore, at the higher bandwidths the readings were more accurate. Based on the results of these two tests (i.e. 1 kc and 200 cps detection bandwidth) and the fact that the 6 cps bandwidth readings were spread about zero, the Rohde and Swartz unit was selected as the noise source. Subsequently, the JPL cognizant engineer recommended an alternate noise power density test as an extension of the scope of work. The results of this effort are summarized in Section G of this Report.

#### Noise Amplifier

The noise amplifier was purchased from RHG Electronics. The amplifier was fabricated in two sections, a preamplifier and power amplifier. Each amplifier has a 3 pole Butterworth response. The

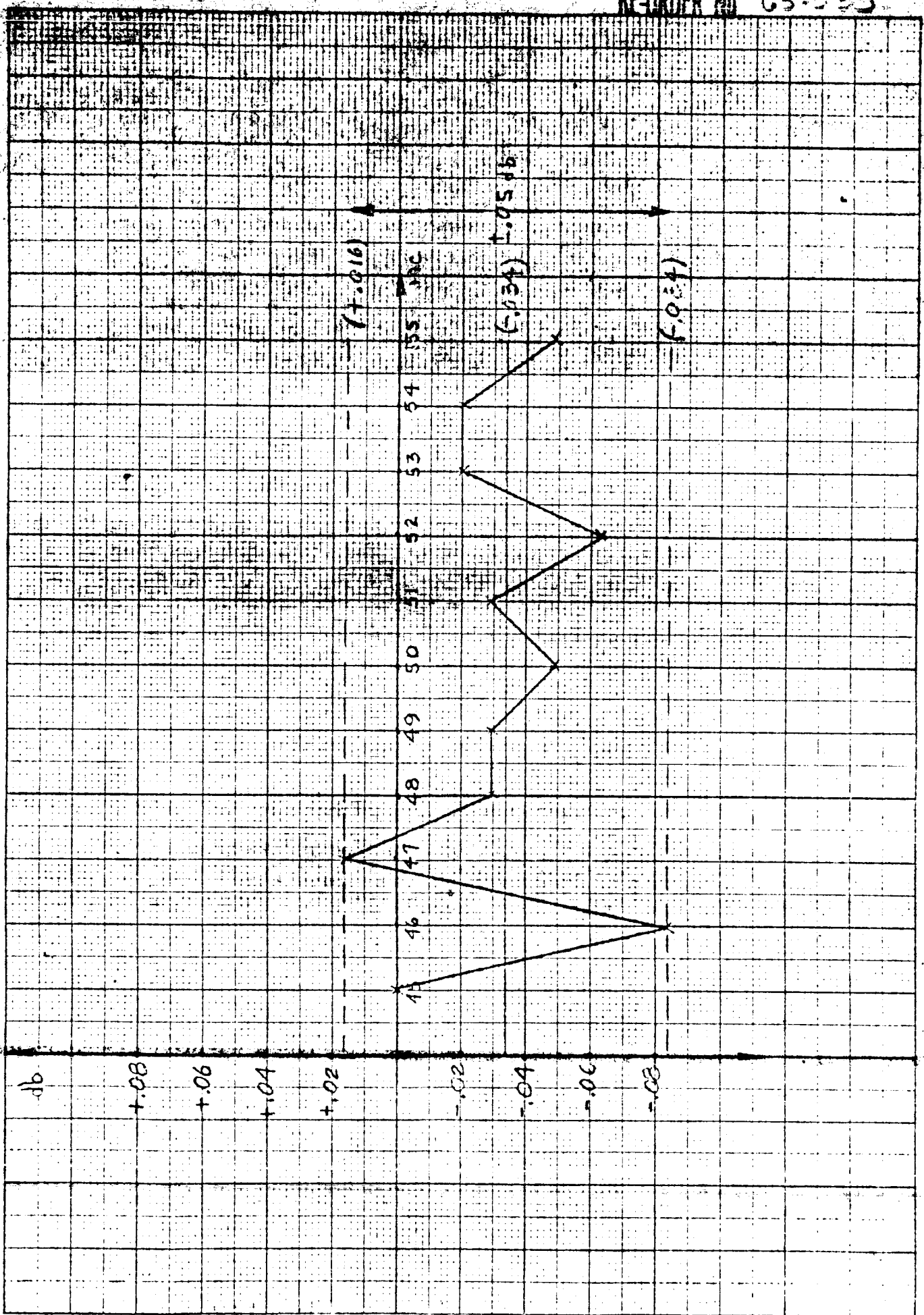


Figure 4 ROHDE SCHWARTZ TEST RESULTS  
Spectral Density 45 to 50 Hz (2 Hz band)  
- 12 -

preamplifier has 10db of gain control. The noise figure is 3db and power gain 115db reduced to 112db by a 3db pad between the preamplifier and power amplifier. The linearity of the amplifier is shown in Figure 7. The third order intermodulation of two tones ( $2f_1 - f_2$ ) and the resulting products that fall within the passband were measured at nominal power output (+ 10dbm) and 6db above and below nominal. The resulting pass-band intermodulation power is indicated by Table I.

Nominal Output + 10 DBM

	44mc	50mc	56mc
6DB above nominal	Ref.	Ref.	-32DB
nominal	Ref.	Ref.	-45DB
6DB below nominal	Ref.	Ref.	-57DB

Table I. Noise Amplifier Intermodulation Data

The passband intermodulation power contribution is 1/1000 the fundamental.

c. Noise Filter

A five pole Butterworth noise filter was synthesized with the following characteristics:

(1) Passband	46 to 54 mc
(2) Ripple in passband	+ 0.05DB
(3) Insertion loss	0.85DB
(4) VSWR	1.1

The filter was fabricated and the out of band rejection plotted as shown by Figure 8. The inband response was measured with the Weinschel Dual Channel System (resolution .01DB) and is illustrated by Figure 9.

The noise bandwidth was computed by graphical integration of an expanded response curve and found to be 15.05 mc.

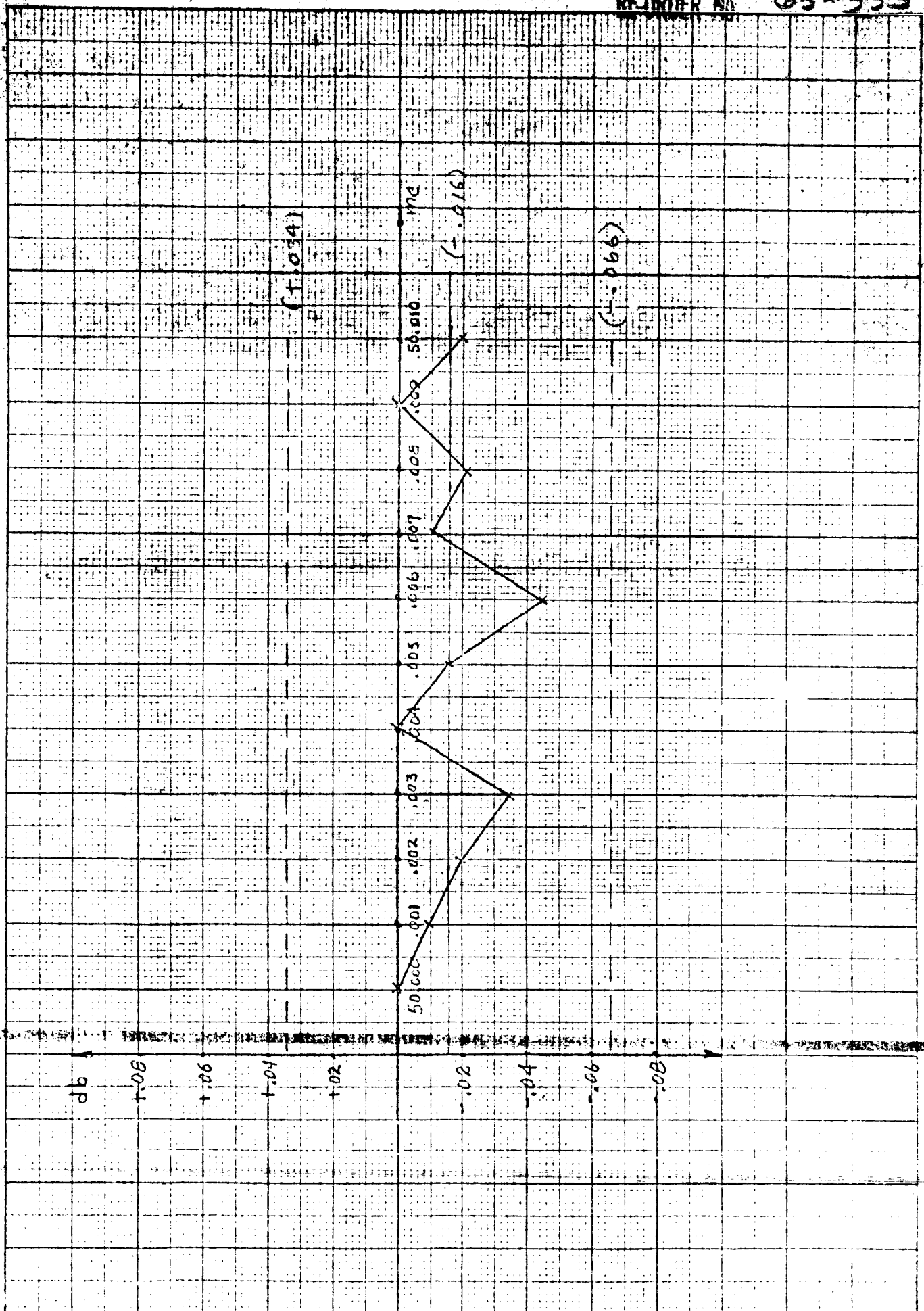
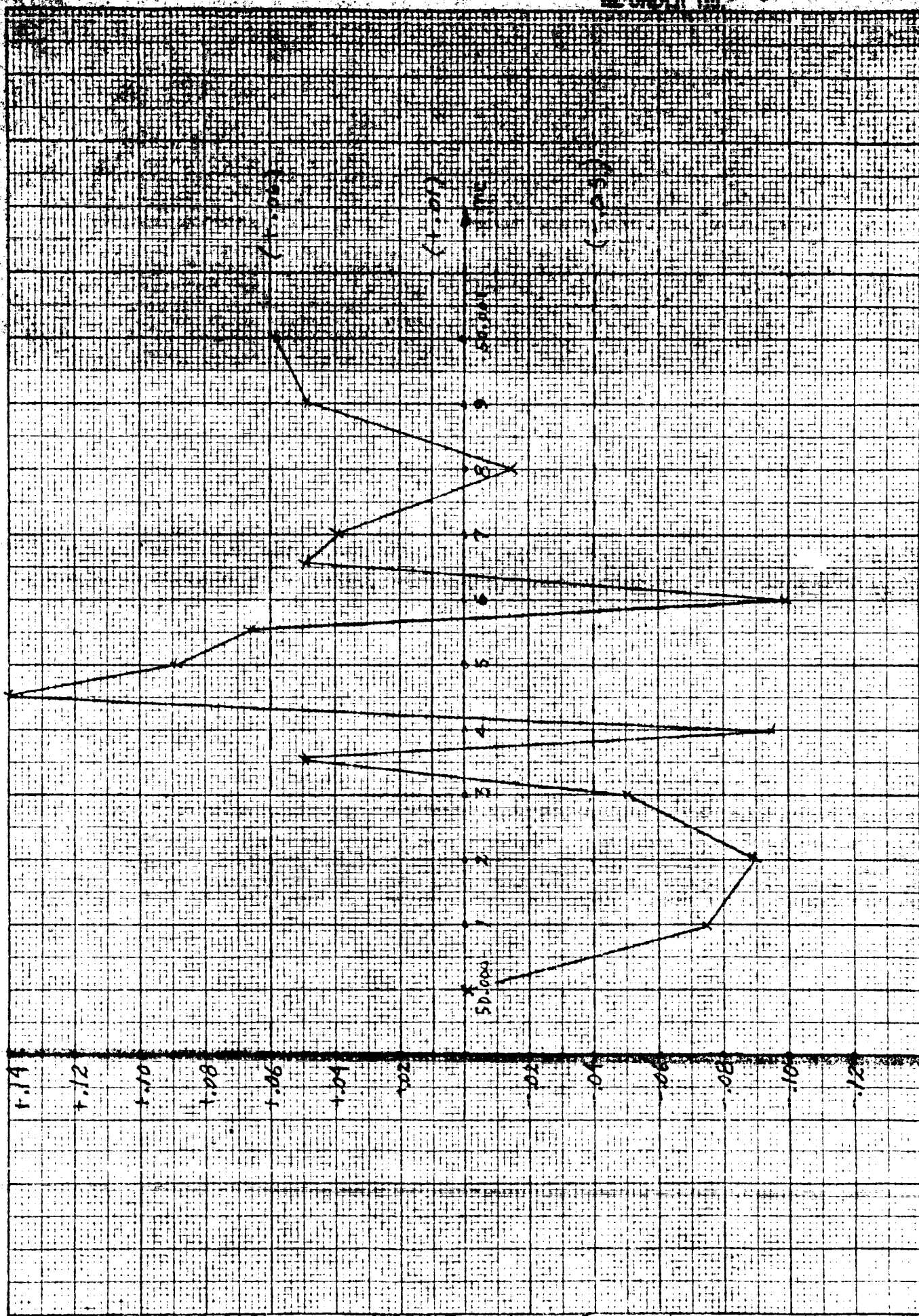


Figure 5 ROHDE-SCHWABE TEST RESULTS  
Spectral Density 50,000 to 50,010 Hz (1 Hz steps)  
- 14 -



ROHDE - SCHWARTZ TEST RESULTS  
Figure 6 Spectral Density 50,000 to 50,010 MC (100 cps steps)



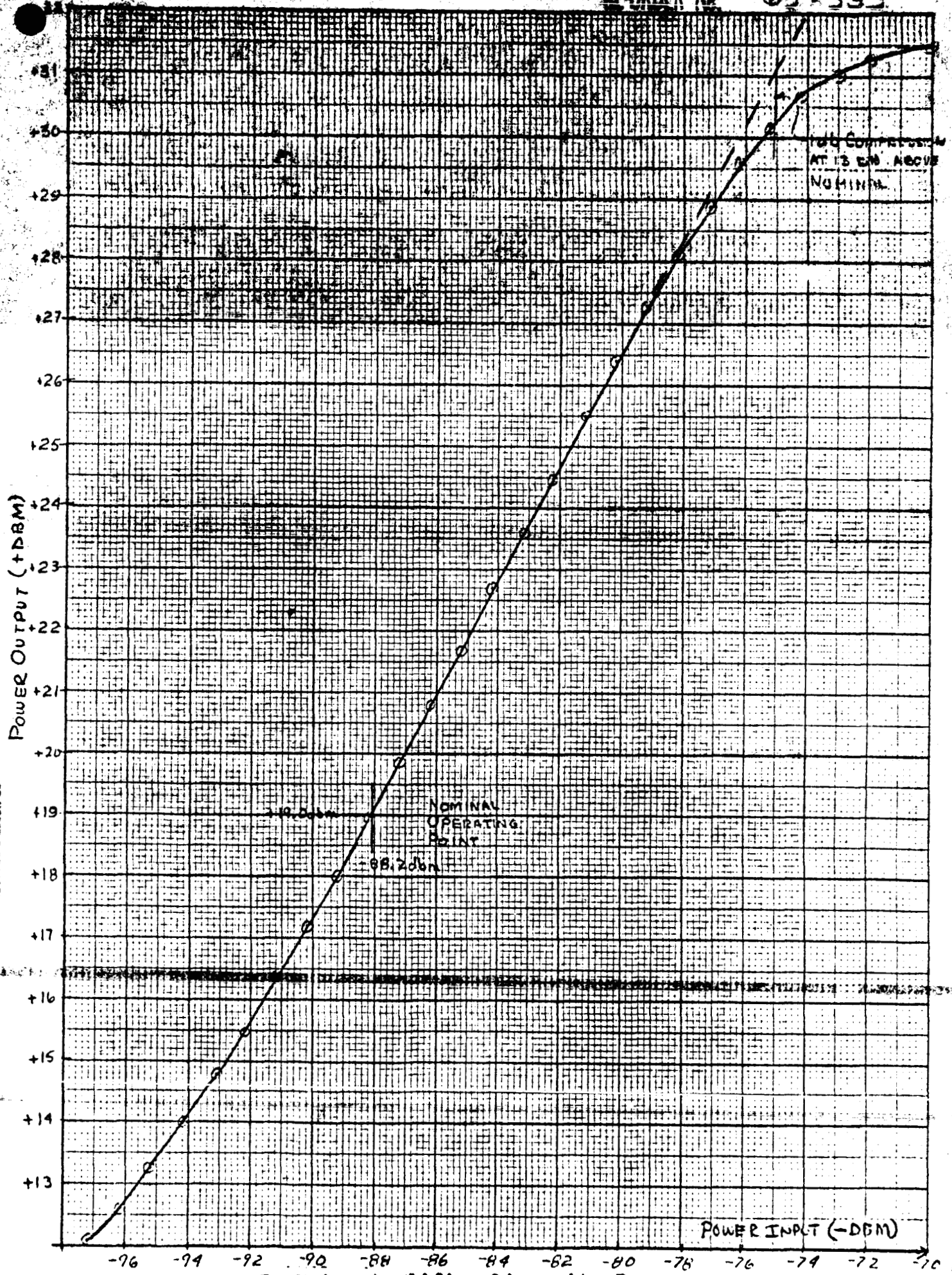


Figure 7. Noise Amplifier Linearity Response - 16 -

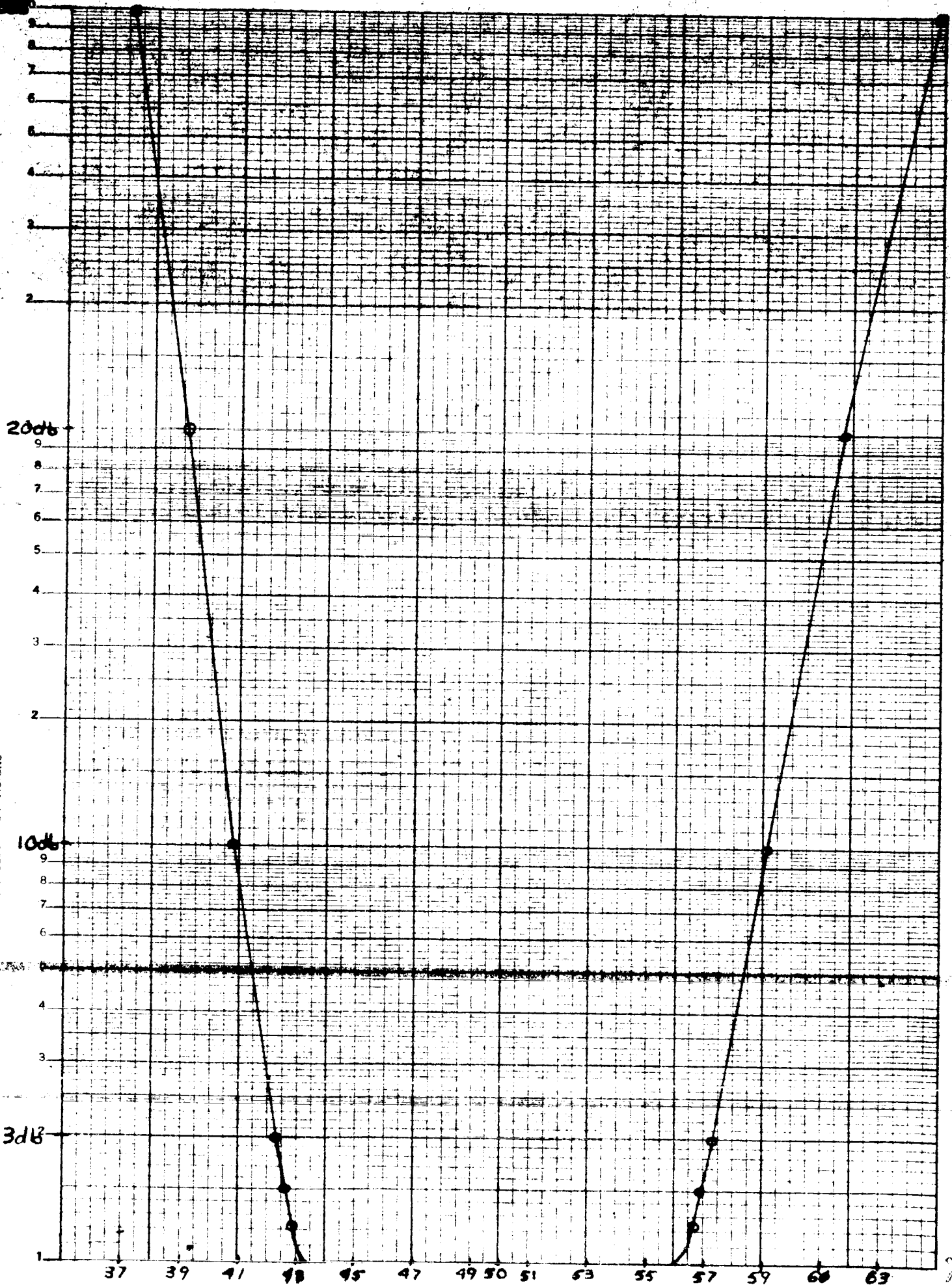


Figure 8. Noise Filter Bandwidth (mcs) - 17 -



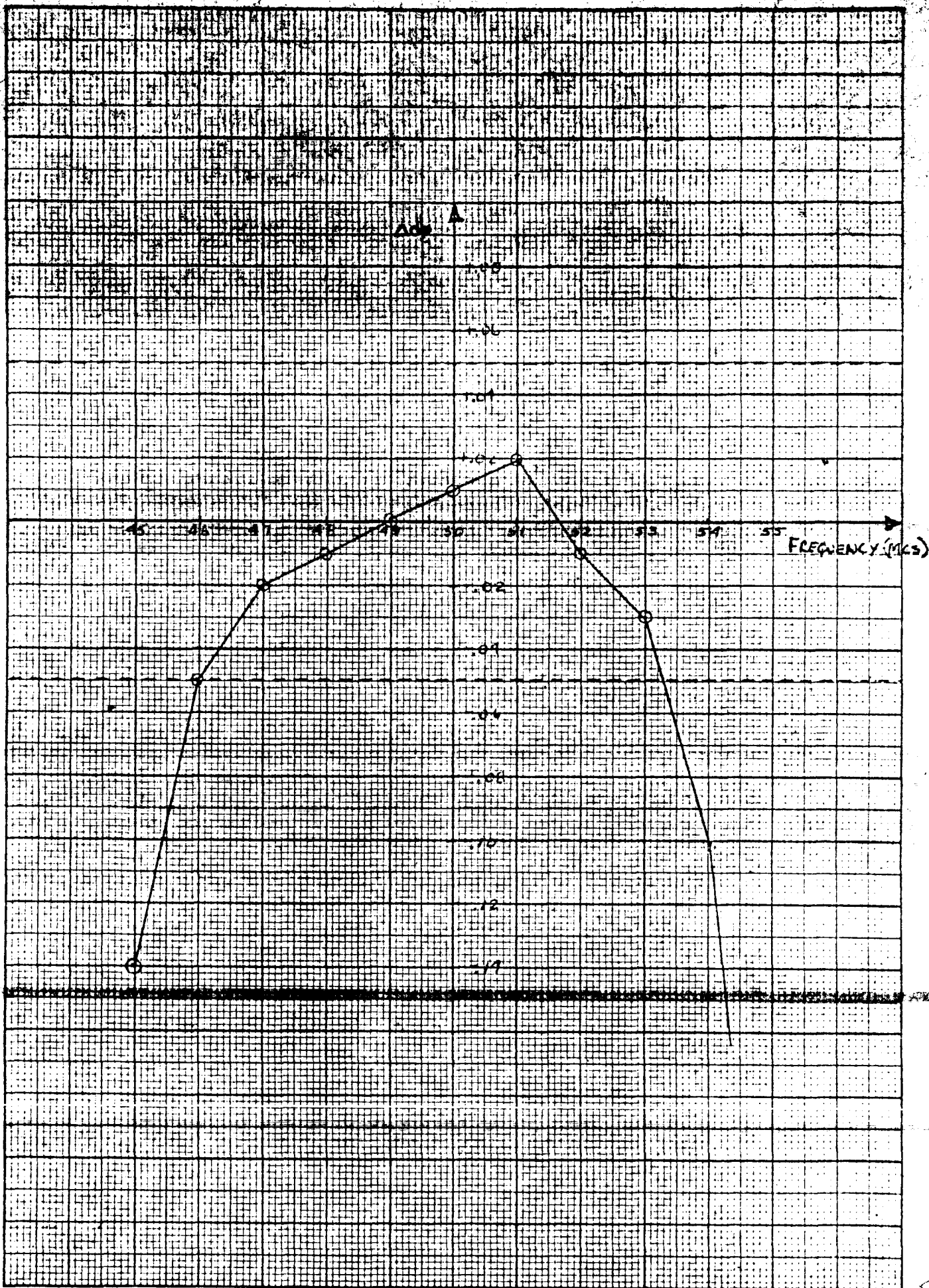


Figure 9. Noise Filter Passband Response

The noise filter and noise amplifier were cascaded and the overall response retested at nominal noise amplifier AGC voltage. The Noise Amplifier/Filter continuation inband response variation was measured to be within  $\pm 0.05$  DB from 44.6 to 53.6 mc. The resulting response is shown in Figure 10.

## 2. S/N Summer Test Results

### a. Test Results

The Linear S/N Summer was tested in accordance with the requirements JPL Spec. GPG-150AZ-DSN par. 3.5.3. The following test measurements were conducted:

- (1) Noise Amplifier/Noise filter frequency response
- (2) Intermodulation
- (3) Linear Summation
- (4) Average S/N Accuracy
- (5) S/N Repeatability

The noise amplifier/filter frequency response tests were discussed earlier in this report. Aside from the intermodulation tests performed on the noise amplifier referenced earlier an intermodulation test of the S/N Summer noise channel was conducted. The results of that test are shown in Table II.

Input Frequency  $f_1 = 50$  MC at -5 dbm

Input Frequency  $f_2 = 53$  MC at -5 dbm

$(2f_1 - f_2) = 47$  MC

Nominal Output -2 dbm

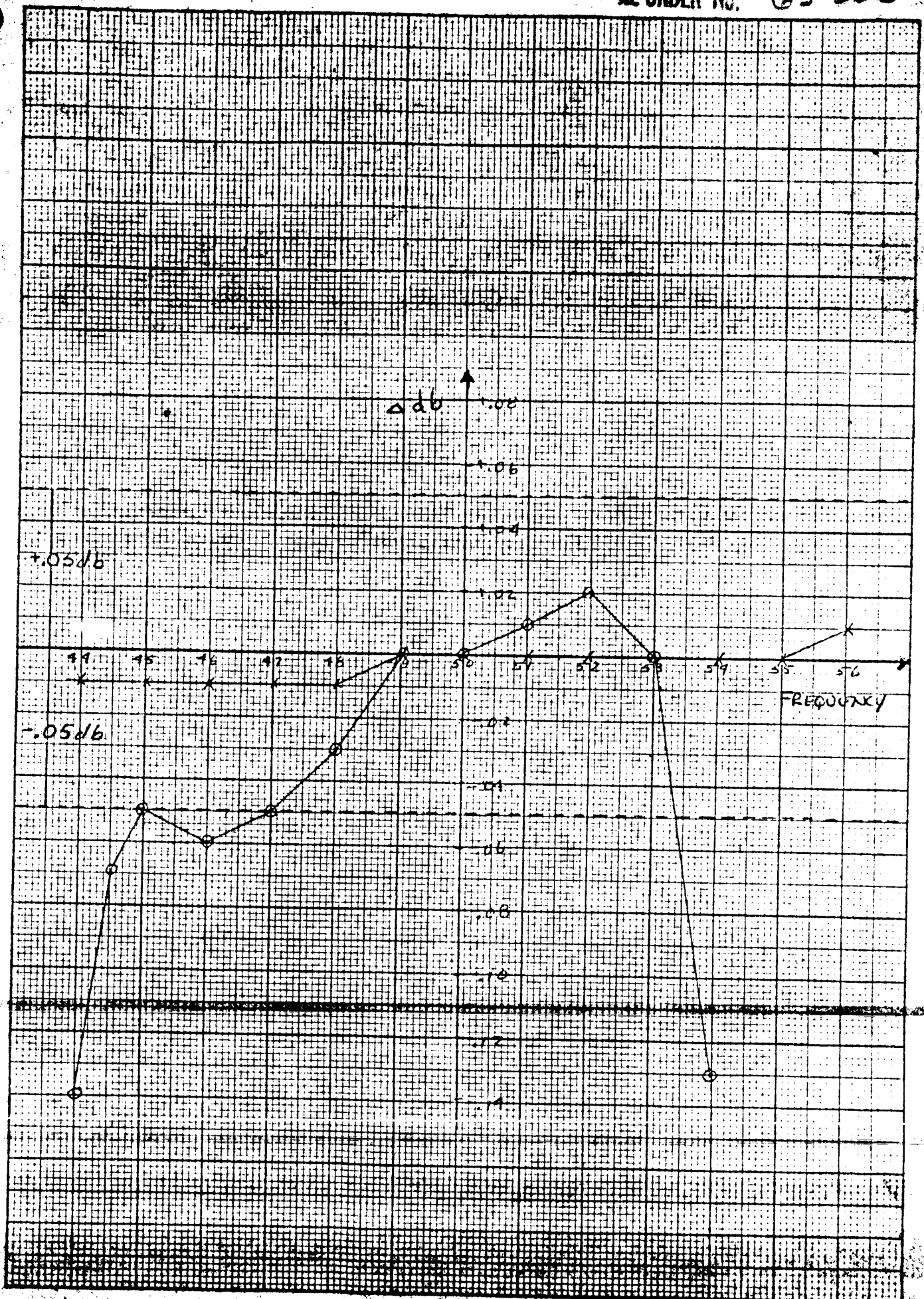


Figure 10. Noise Amplifier Point by Point Freq. Response - 20-

	50 MC	53 MC	47 MC
Nominal	-5 dbm	-5 dbm	30 db down
3db Above Nominal	-2 dbm	-2 dbm	30 db down
6db Above Nominal	+1 dbm	+1 dbm	26 db down

Table II. Noise Channel Intermodulation Test Results

As shown the inband intermodulation components of the composite noise channel are 6DB higher than the intermodulation components of the noise amplifier alone.

A verification test of the linear summing at the output of the S/N Summer is shown in Figure 11. The output of each channel was adjusted for equal power levels, then with the linear S/N summer operating in its normal operating condition of closed loop, each channel was separately varied using the precision attenuators and the change in output power was recorded. The change in power output was compared with the theoretical change to get a measure of the linear summing. These readings are shown in Table III.

For the average S/N measurement, the linear S/N Summer was set up as shown in Figure 12. With the measurement system connected to the output of the summer as shown in Figure 11, the power level of each channel was adjusted such that at the output of the amplifier in the test set-up, the Signal Power  $P_s$  was 10db down from the Noise Power  $P_n$ . At the output of the summer itself, the Noise Power  $P_n$  is 20db greater than the Signal Power  $P_s$  because the bandwidth of the noise channel is 15 MC whereas the test amplifier bandwidth is approximately 1.5 MC.

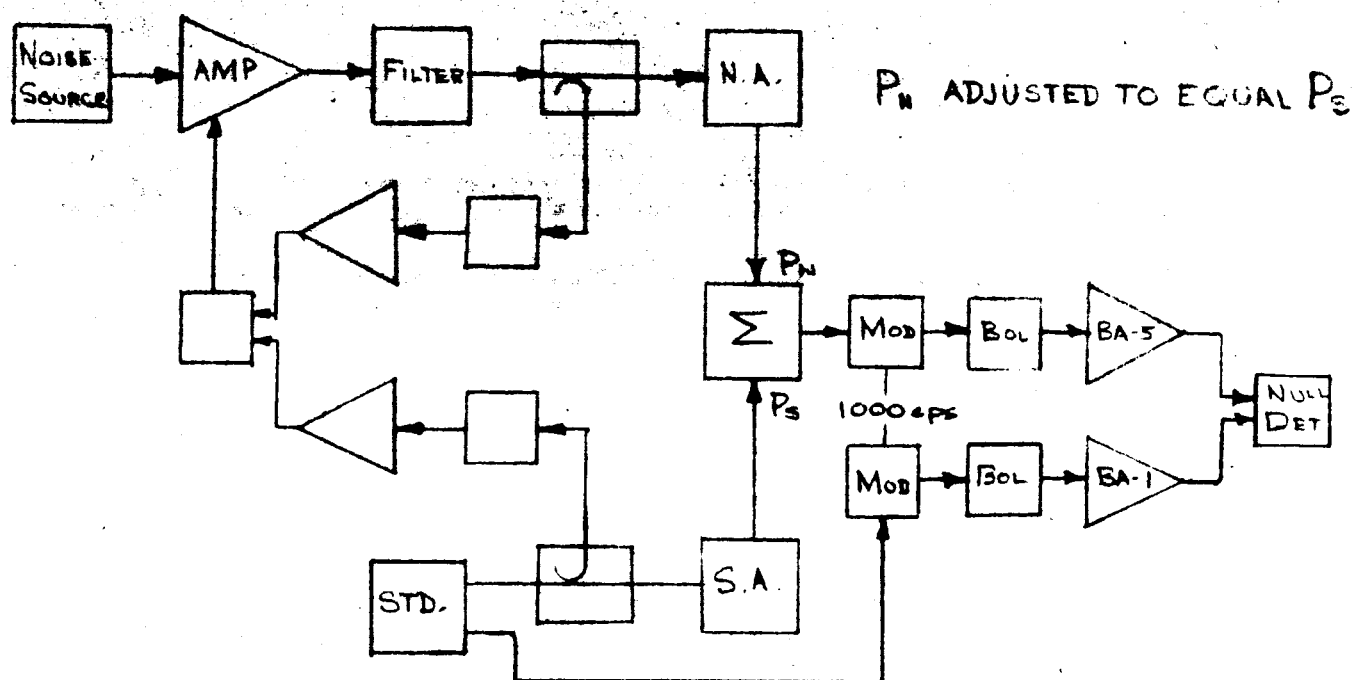


FIGURE 11. LINEAR SUMMING TEST SET-UP

N.A. SET AT 0.00			
S.A.	THEOR. CHANGE	$\Delta db$	ERROR
0.00	REF	—	—
1.00	.470	.460	-.010
2.00	.887	.870	-.017
3.00	1.246	1.240	-.006
5.00	1.815	1.800	-.015
10.00	2.596	2.565	-.031
20.00	2.967	2.930	-.037
50.00	3.010	2.970	-.040

S.A. SET AT 0.00			
N.A.	THEOR. CHANGE	$\Delta db$	ERROR
0.00	REF	—	—
1.00	.470	.460	-.010
2.00	.887	.870	-.017
3.00	1.246	1.230	-.016
5.00	1.815	1.790	-.025
10.00	2.596	2.565	-.031
20.00	2.967	2.930	-.037
50.00	3.010	2.975	-.035

REFERENCE :  $P_N = P_S$

$$P_{REF} = P_N + P_S = 2P$$

$$\therefore P_{OUT} = 10 \log \frac{2P}{P_S + \Delta P_S} \quad (\text{FOR N.A. SET AT 0.00})$$

$$P_{OUT} = 10 \log \frac{2P}{P_S + \Delta P_N} \quad (\text{FOR S.A. SET AT 0.00})$$

TABLE III LINEAR SUMMING TEST RESULTS

The resulting  $P_n$  and  $P_s$  at the test amplifier output was -10 dbm and -20 dbm respectively. All possible combinations of S/N Ratios with the above set-up are displayed in the matrix shown in Table IV.

In the measurement set-up, the combination of the attenuator and amplifier A had the range of 0 to 30db of attenuation. That is, for A set at 30db,  $P_n = -10$  dbm and  $P_s = -20$  dbm; for A set at 0db,  $P_n = +20$  dbm and  $P_s = +10$  dbm. The matrix was divided into 4 quadrants such that; in quadrant I, A was set to 30db of attenuation; in quadrant II, A was set to 0 for the signal attenuator (SA) settings and 30db for the noise attenuator (NA) settings; in quadrant III, A was set to 0db for the NA settings and 30db for the SA settings, and finally; in quadrant IV, A was set to 0db for both the NA and the SA settings. In the above manner, it was possible to test every possible S/N setting.

With the range of 50db for each attenuator and the smallest increment of each of .1db, there are 500 possible settings on the NA and the SA or in combination  $25 \times 10^4$  possible S/N settings. Since this was virtually impossible to test in total, random settings were generated in each quadrant and a total of 10 readings were taken from each quadrant plus the corner settings of each, i.e. 0.0 - 0.0, 0.0 - 50.0, 50.0 - 0.0 and 50.0 - 50.0.

From the results of these tests, the mean, variance, and standard deviation of each quadrant was calculated. These readings and calculations are shown in Table V. By comparison, each quadrant was found to be a sub-set of the total population, and a mean, variance and standard deviation was calculated for all the readings. From this mean and

		① -45dbm ② -45dbm						① -45.1dbm ② -10dbm						
# P <sub>n</sub>	S.A.	-20dbm												-70dbm
	N.A.	0.0	0.1	0.2		24.8	24.9	25.0	25.1	25.2	25.3	49.8	49.9	50.0
① -10dbm ② -10dbm	0.0	-10.0	-10.1	-10.2		-34.8	-34.9	-35.0	-35.1	-35.2	-35.3	-59.8	-59.9	-60.0
	0.1	-9.9	-10	-10.1		-34.7	-34.8	-34.9	-35.0	-35.1	-35.2	-59.7	-59.8	-59.9
	0.2	-9.8	-9.9	-10		-34.6	-34.7	-34.8	-34.9	-35.0	-35.1	-59.6	-59.7	-59.8
QUADRANT I						QUADRANT II								
① -35dbm ② -35dbm	24.9	+14.9	+14.8	+14.7		-9.9	-10	-10.1	-10.2	-10.3	-10.4	-34.9	-35.0	-35.1
	25.0	+15.0	+14.9	+14.8		-9.8	-9.9	-10	-10.1	-10.2	-10.3	-34.8	-34.9	-35.0
① -55.1dbm ② -5dbm	25.1	+15.1	+15.0	+14.9		-9.7	-9.8	-9.9	-10	-10.1	-10.2	-34.7	-34.8	-34.9
	25.2	+15.2	+15.1	+15.0		-9.6	-9.7	-9.8	-9.9	-10.0	-10.1	-34.6	-34.7	-34.8
	25.3	+15.3	+15.2	+15.1		-9.5	-9.6	-9.7	-9.8	-9.9	-10.0	-34.5	-34.6	-34.7
QUADRANT III						QUADRANT IV								
① -60dbm ② -30dbm	49.8	+39.8	+39.7	+39.6		+15.0	+14.9	+14.8	+14.7	+14.6	+14.5	-10.0	-10.1	-10.2
	49.9	+39.9	+39.8	+39.7		+15.1	+15.0	+14.9	+14.8	+14.7	+14.6	-9.9	-10.0	-10.1
	50	+40.0	+39.9	+39.8		+15.2	+15.1	+15.0	+14.9	+14.8	+14.7	-9.8	-9.9	-10.0

\* The power levels indicated at the beginning and end of the quadrants of the signal attenuator row and noise attenuator column are:  
(1) the power levels at the output of the summer referenced to the LMC bandwidth of the amplifier A, and (2) the power levels into the bolometer.

Table IV. Matrix of Average S/N Reading



QUADRANT I					
NO.	S.A.	N.A.	S/N CALC	S/N MEAS	$\Delta db$
1	.3	3.2	-7.1	-7.17	-.07
2	7.3	4.1	-13.2	-13.2	00
3	11.6	24.3	+2.7	+2.70	00
4	13.1	5.9	-17.2	-17.30	-.10
5	12.6	29.3	+6.7	+6.63	-.07
6	4.7	11.4	-3.3	-3.40	-.10
7	13.7	26.1	+2.4	+2.32	-.08
8	16.5	22.2	-4.3	-4.27	+.03
9	13.4	27.8	+4.2	+4.07	-.13
10	8.3	19.9	+1.6	+1.56	-.04
CORNER	0.0	0.0	-10.0	-9.91	+.09
$n=11$ $\bar{X} = -.043db$ $V = .00434$ $\sigma = .0659$					

QUADRANT II					
NO.	S.A.	N.A.	S/N CALC	S/N MEAS	$\Delta db$
1	38.4	28.4	-20	-20.05	-.05
2	49.5	24.3	-36.3	-35.28	+.02
3	29.7	29.3	-10.4	-10.44	-.04
4	23.9	7.8	-26.1	-26.19	-.09
5	21.8	22.9	-8.9	-8.97	-.07
6	39.0	24.0	-25.0	-25.09	-.09
7	45.2	28.0	-27.2	-27.12	+.08
8	39.7	20.8	-28.9	-28.98	-.08
9	48.0	0.9	-57.1	-56.94	+.07
10	45.7	29.6	-26.1	-26.12	-.02
CORNER	50.0	0.0	-60.0	-60.01	-.01
$n=11$ $\bar{X} = -.0254db$ $V = .00373$ $\sigma = .0611$					

QUADRANT III					
NO.	S.A.	N.A.	S/N CALC	S/N MEAS	$\Delta db$
1	10.1	36.5	+16.4	+16.35	-.05
2	1.9	32.1	+20.2	+20.19	-.01
3	18.8	39.9	+11.1	+11.06	-.04
4	14.9	10.6	+15.7	+15.63	-.07
5	9.6	47.2	+27.6	+27.66	-.04
6	12.5	33.2	+10.7	+10.65	-.05
7	7.5	30.3	+12.8	+12.74	-.06
8	19.3	31.6	+2.3	+2.29	-.01
9	11.9	30.9	+9.0	+9.0	00
10	1.3	43.1	+31.8	+31.89	+.09
CORNER	0.0	50.0	+40	+40.05	+.05
$n=11$ $\bar{X} = -.0173db$ $V = .00242$ $\sigma = .0492$					

QUADRANT IV					
NO.	S.A.	N.A.	S/N CALC	S/N MEAS	$\Delta db$
1	35.2	34.8	-10.40	-10.50	-.10
2	21.2	48.0	+16.80	+16.87	+.03
3	29.9	45.1	+5.20	+5.22	+.02
4	36.4	44.0	-2.40	-2.34	+.06
5	44.7	31.8	-22.9	-22.86	+.04
6	37.3	31.7	-15.60	-15.66	-.06
7	45.0	38.4	-16.60	-16.70	-.10
8	30.3	33.7	-6.60	-6.72	-.12
9	35.6	36.0	-9.60	-9.74	-.14
10	30.2	36.1	-4.10	-4.25	-.15
11	36.3	39.8	-6.50	-6.60	-.10
CORNER	50.0	60.0	-10.0	-10.05	+.05
$n=12$ $\bar{X} = -.0475$ $V = .00654$ $\sigma = .0809$					



standard deviation a 95% confidence interval with 5% tolerance limits was applied and it was found that no more than 5% of the readings would fall outside of  $\pm .155\text{db}$ .

$$N = 45 \text{ Readings}$$

$$\sum x_a = 1.51$$

$$\bar{x} = .0336\text{db}$$

$$N_{\text{VAR}} = \sum_{a=1}^N x_a^2 - N\bar{x}^2$$

$$V = .0042$$

$$\sigma = .065$$

Therefore with 95% confidence that 95% of the readings fall within the limits:

$$\bar{x} + K(.065) \quad X \quad \bar{x} - K(.065)$$

$$-.034 + (2.41)(.065) \quad X \quad -.034 + (2.41)(.065)$$

$$-.190\text{db} \leq X \leq +.123\text{db}$$

The repeatability was tested by selecting eight S/N settings which utilized as many of the attenuators inside the precision attenuators (NA and SA) and repeating these S/N settings continually at a random rate over a four hour period. By using only eight S/N settings, it was possible to repeat each setting thirteen times for a total of 104 readings. In order to cover a wider range on both the NA and SA, the 20db pad was removed from the signal channel such that the signal level equalled the noise at the output of the summer when both the SA and NA were set at the same setting. In order to eliminate as much drift and

instability in the test equipment, the test amplifier was removed and the readings were made at the noise bandwidths of 15 MC with a test set-up similar to that of Figure 12.

The data compiled for this measurement is shown in Table VI. The largest difference in readings for any one setting was .023db. This data was analyzed and the mean, and standard deviation for each of the eight readings was computed. The 95% confidence level at 5% tolerance limits was applied to each of these settings to get a measure of S/N setting repeatability. In the worst case it can be stated with 95% confidence that no more than 5% of the readings would repeat outside  $\pm .024$ db. The calculations of the mean, standard deviation and 5% tolerance limits are shown at the right of Table VI.

Each group of the eight S/N settings was treated as a subset of the total readings. A mean and standard deviation was computed for each of these subsets. These calculations are shown at the bottom of Table VI. The off-set or mean for each of the set of readings was found to be an error in the setting up of the initial conditions. That is in setting the signal power equal to the noise power by first setting a reference level in the measurement system from one of the channels and then duplicating this reference from the other channel. The problem appeared to be distortion introduced by the 1000 cps modulator for when the two channels were balanced using a power meter, a different mean was achieved. This is a static off-set which created no problem other than operating about some value other than zero. The relation between S/N settings was unchanged for different off-sets.

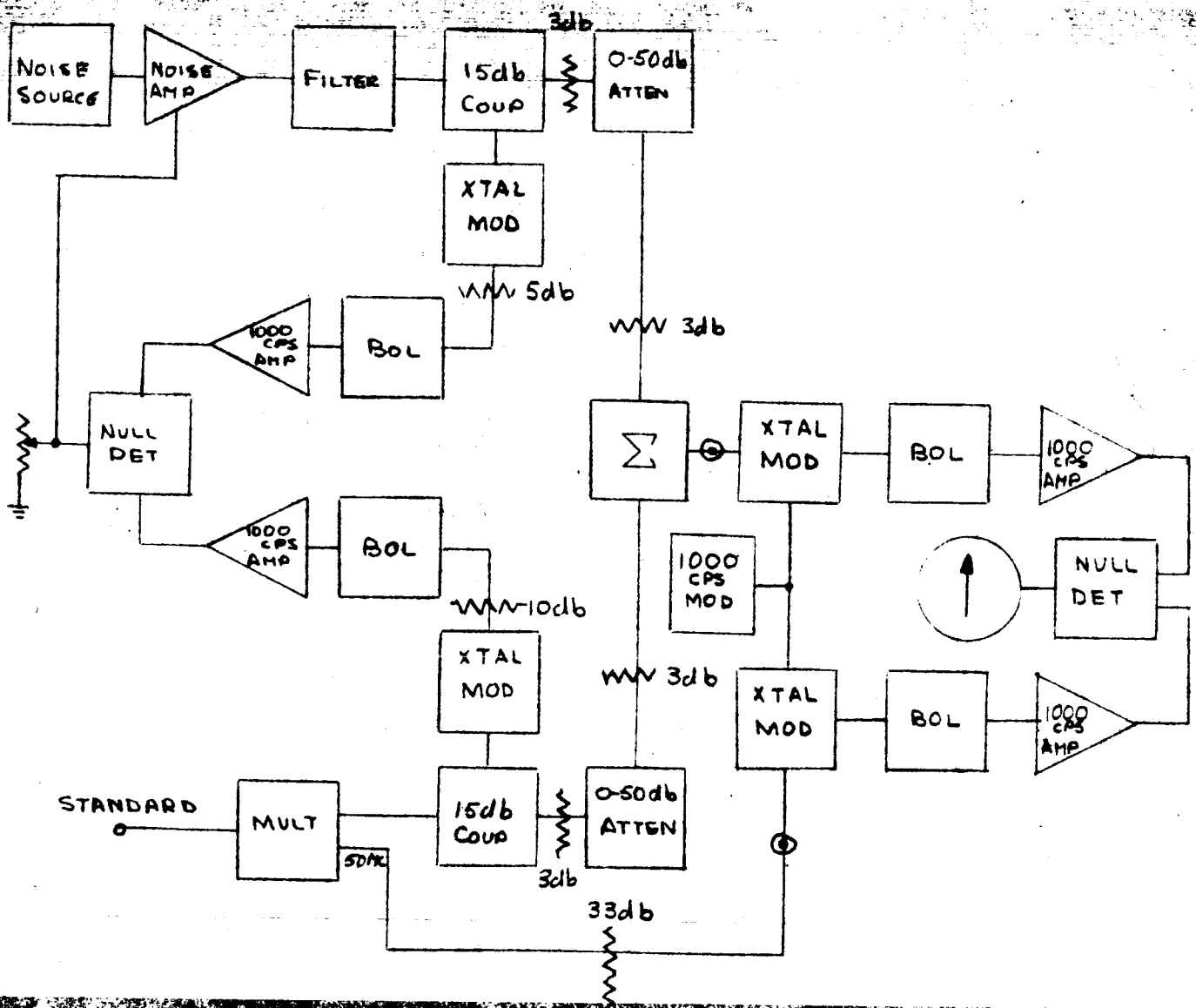


Figure 12 Feedback Control Loop Test Set-Up

SIGNAL NOISE ATTEN	3/N BW = 15Mc	DEVIATION FROM CALCULATED 3/N SETTINGS (DB)													MEAN $\bar{x}$	STD DEV $\sigma$	6% TOL
		1	2	3	4	5	6	7	8	9	10	11	12	13			
7.3	4.1	-0.05	0.000	-0.010	0.000	-0.005	-0.010	-0.010	-0.015	-0.012	-0.014	+0.001	0.000	-0.007	0.0166	.0056	±.0124
8.0	18.2	-0.055	-0.050	-0.055	-0.060	-0.065	-0.070	-0.060	-0.064	-0.069	-0.073	-0.058	-0.063	-0.060	.023	.0064	±.020
13.1	5.9	-0.040	-0.040	-0.040	-0.045	-0.040	-0.040	-0.050	-0.055	-0.055	-0.043	-0.033	-0.045	-0.033	.022	.0070	±.022
7.1	19.9	-0.080	-0.075	-0.095	-0.095	-0.090	-0.090	-0.080	-0.096	-0.098	-0.090	-0.083	-0.090	-0.097	.023	.0075	±.024
19.2	14.5	-0.040	-0.035	-0.035	-0.045	-0.040	-0.050	-0.050	-0.045	-0.045	-0.036	-0.036	-0.045	-0.042	.015	.0053	±.017
15.0	13.2	-0.065	-0.060	-0.065	-0.060	-0.055	-0.065	-0.066	-0.073	-0.070	-0.054	-0.065	-0.067	-0.062	.019	.0054	±.017
4.5	11.4	-0.090	-0.080	-0.085	-0.095	-0.090	-0.095	-0.087	-0.098	-0.099	-0.083	-0.078	-0.090	-0.084	.021	.0067	±.021
0.3	3.2	-0.040	-0.045	-0.045	-0.050	-0.050	-0.050	-0.048	-0.050	-0.050	-0.044	-0.047	-0.054	-0.045	.014	.0037	±.011
MEAN $\bar{x}$		.0519	.0481	.0538	.0563	.0544	.0588	.0564	.0620	.0623	.0546	.0499	.0568	.0547			
STD DEV $\sigma$		.0269	.0252	.0260	.0304	.0281	.0276	.02361	.0317	.0287	.0257	.0247	.0289	.0289			

Table VI. 3/N Deviation from Calculated 3/N Settings

The change in the means of the 13 sets of S/N readings over the 1/4 hour measurement period is a measure of the drift of the linear S/N Summer plus the measurement system. The mean of these 13 means is .0054db with a variance of  $1.717 \times 10^{-5}$  and a standard deviation of .004. From this data it can then be stated that with 95% confidence and 5% tolerance limits, the system would not drift more than  $\pm .013$ db. This includes the drift of the measurement system and is well within the specification requirement of  $\pm 0.1$ db/1/4 hour period for the signal power and  $\pm 0.1$ db/1 hour period for the noise power.

b. Conclusion

The test results of the Linear S/N Summer satisfy all of the specification requirements outlined in paragraph 3.5.3 of the JPL Specification GPG-15062-DSN. Using random sampling techniques, 40 S/N Measurements from a population of 250,000 S/N settings were made and found to be accurate within  $\pm .155\text{db}$ . The specification calls for  $\pm .3\text{db}$  over this 100db dynamic range. Repeatability over a four hour period was measured to be between .011 and .024db. The overall drift of the Linear S/N Summer is  $\pm .013\text{db}$  compared with the specification of  $\pm 0.1\text{db}$  each, for the noise source, the signal source and the power monitor.

The frequency response of the noise channel was measured at room temperature to be flat within  $\pm .05\text{db}$  from 44.6 to 53.6 mc.

c. PM/AM Subsystem

The PM/AM Subsystem as outlined in Figure 1 consists of a PM and AM Transmitter, PM Receiver and Phase Noise Instrumentation. The applicable appendices are listed as follows: 1) Appendix D, Locked oscillator phase modulator 2) Appendix E, Deviation Multiplication Phase Modulator 3) Appendix F, PM Receiver 4) Appendix G, Phase Noise Instrumentation. The following sections of the final report constitute a summary of these appendices. Note that two appendices apply to the Phase Modulator and that the Locked oscillator Phase Modulator is recommended for the R.F. Test Console.

# 1. Locked Oscillator Phase Modulator

The detailed results of the Locked Oscillator Phase Modulator investigation are listed in Appendix D. The following constitutes a summary of that effort.

## a. Summary

Design parameters which enable linear phase modulation of a locked oscillator by complex video signals are established by analysis. The driving signal is summed with the phase error to deviate the locked oscillator as outlined in the block diagram of Figure 13, thereby producing a PM output at the carrier frequency.

The analysis indicates that the system is feasible provided that (1) a phase detector with a linear  $\frac{\Delta E}{\Delta \theta}$  transfer is implemented. (2) The linearity and time constant of the VCO is adequate.

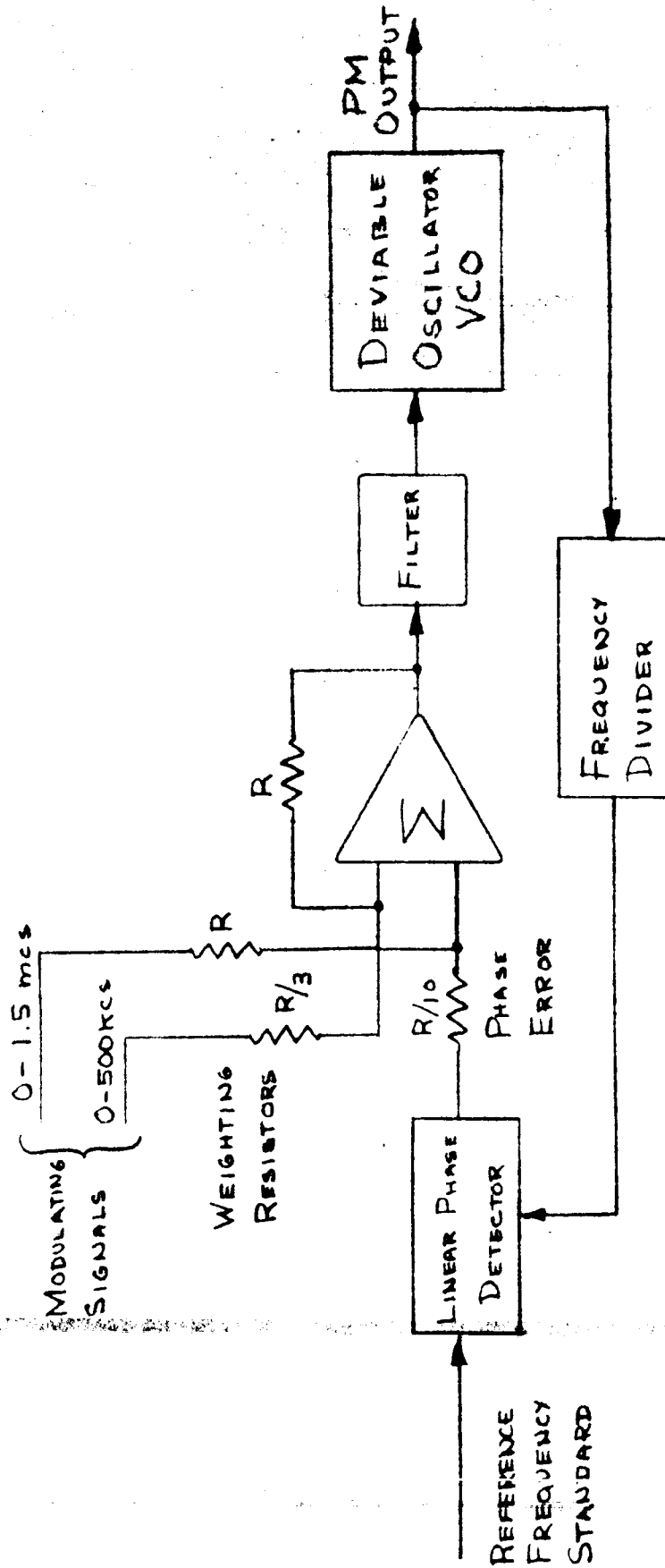


FIGURE 13 BASIC PHASE LOCKED PM MODULATOR



3) A count down frequency divider is used in the feedback channel to compress the phase deviation applied to the phase to within its linear region. 4) The loop filter  $F(s)$  is optimized with regard to rejection of phase detector harmonics, amplitude and phase response of the baseband modulation.

b. Phase Modulator Requirements

The Phase Modulator requirements are summarized as follows:

(1) Summary of Specifications

- |                                  |  |
|----------------------------------|--|
| (a) Transmitter Center Frequency | 50 MC Manually<br>Tunable $\pm$ 500 cps  |
| (b) PM Modes                     | Simultaneous Narrowband/large modulation index plus wideband/small modulation index operation  |
| (c) Frequency Stability          | Short term 1 part in $10^7$ /minute<br>Long term 5 parts in $10^7$ /4 hours  |
| (d) Frequency Response           | $\pm$ 0.1DB from DC to 500 KC<br>$\pm$ 0.5DB from 500 KC to 1.5 MC   |
| (e) Phase Deviation at 50 MCS    | Narrowband Spectrum $\pm$ 3 rad. peak<br>Wideband Spectrum $\pm$ 1 rad peak  |
| (f) Phase Stability              | 1 Degree RMS phase error in TX/RX pair in 2 BLO of 3.0 cps   |
| (g) Fidelity                     | Two tone tests of TX/RX pair<br>Spurious within modulation bandwidth, 40DB below modulated carrier or 50DB below unmodulated carrier |
| (h) Deviation Linearity          | consistent with linearity requirement  |
| (i) Incidental AM                | consistent fidelity requirements   |

(2) Analysis of Requirements(a) Peak Frequency Deviation

The VCO and driving amplifier must have a linear dynamic range of  $\pm 2.0$  mc at 50 mc output frequency.

(b) Spectral Weighting of Modulation Signals

The amplitude levels of the narrowband and wideband modulation spectrums are weighted such that the peak narrowband deviation is  $\pm 3$  radians and the wideband peak deviation  $\pm 1$  radian. The total composite phase deviation is  $\pm 4$  radians.

(c) Fidelity Requirements

The Specification references the TX/RX pair. Equal degradation is allotted the TX and RX. The inband TX intermodulation and spurious objectives is -46DB and -56DB with respect to the modulated carrier and unmodulated carrier respectively.

(3) Summary of Design Objectives(a) Loop Characteristics

- (1) open loop, 6DB/active slope of open loop gain over baseband
- (2) closed loop amplitude response  $\pm 0.1$ DB to 0.5 MCS and 0.5DB to 1.5MCS.
- (3) -50DB rejection at 25 MCS
- (4) -56DB spurious and inband intermodulation
- (5) peak phase deviation 4 rad.

## (b) VCO

- (1) Peak frequency deviation  $\pm 2$  MCS
- (2) Sensitivity  $0.6 \cdot 10^{+6}$   $\frac{\text{cycle}}{\text{volt sec.}}$
- (3) Linearity 2%
- (4) Q  $\approx 12.5$
- (5) Output carrier frequency 50MCS

(c) Phase Detector

- (1)  $\frac{E_o}{\theta_i - \theta_o}$  transfer Linear
- (2) Linearity 5% (1 radian deviation)
- (3) Phase Error Range  $\pm 1$  radian
- (4) Sensitivity 1 volt/radian

(d) D.C. Amplifier

- (1) Gain 20DB
- (2) Linearity 0.1%
- (3) Output Voltage Range  $\pm 10V$
- (4) Equivalent Carrier Frequency 15MC
- (5) Drift 100uv/wk
- (6) Feedback Divider Ratio  $N = 4$
- (7) Estimated Loop Transport Lag 20 nanosec.

c. Loop Design Considerations

Fundamental relationships of phase lock loops as applied to the Locked oscillator Phase Modulator are reviewed in this section.

(1) Optimization Criteria

The loop design is dependent on the application. The designer has the choice of optimizing one or more of the following parameters at the expense of others a modulation error b Intermodulation c transient response d maximally flat frequency response with large out of band rejection e optimally flat group delay (with less out of band group delay). The loop operates in a noise free environment; therefore, minimization of noise error is not a major consideration. Loop stability is not a major consideration but constitutes a limiting factor of transient error.

A summary of the loop designs considered is stated as follows:  
we select the criteria for a locked oscillator phase modulator to be the minimization of modulation error and intermodulation by use of a "maximally" flat delay response. The loop gain and bandwidth must be consistent with the modulation spectrum and have adequate rejection of spurious harmonics generated by the loop multiplier. The various loop designs considered are summarized in the following sections. The loop designs were synthesized and the open loop amplitude and phase response and closed loop amplitude, phase and deviative of phase (group delay) computed on the SDS-910 computer.

## (2) Fundamental Form-Phase Margin Loop Design

A simplified mathematical model of the Locked Oscillator Phase Modulation is shown in Figure 14. The transfer function of output phase to modulation input is listed by equation 1.

$$\frac{\Delta \theta_o(s)}{V_m(s)} = \frac{K_\alpha K_{vco} F_1(s)}{s\left(\frac{s}{\omega_i} + 1\right) \left[1 + \frac{K_m K_\alpha K_{vco} F_1(s)}{N s\left(\frac{s}{\omega_i} + 1\right)}\right]} \quad (1)$$

Let  $K_v = \frac{K_A K_D K_{vco}}{N} \quad (2)$

Then (3)

$$\frac{\Delta \theta_o(s)}{V_m(s)} = \frac{N}{K_m} \frac{1}{\frac{s}{K_v} \left(\frac{s}{\omega_i} + 1\right) F_1(s)} + 1$$

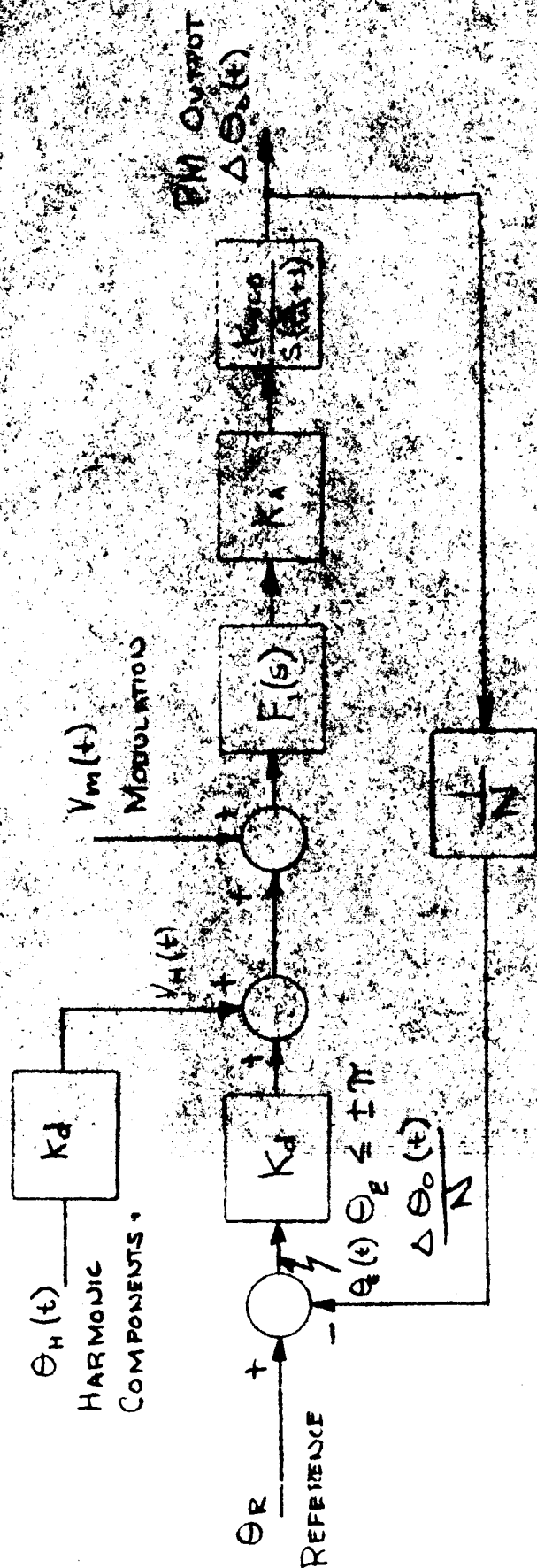


FIGURE 14 ELEMENTARY PLC-PHASE MODULATOR EQUIVALENT DIAGRAM

Ideally the output phase,  $\Theta_o$ , is a linear function of  $V_m$  over the baseband; however,  $F_1(s)$  must be arranged to sufficiently reject the harmonics rejected by the loop multiplier. Initially  $F_1(s)$  was considered as a simple pole at  $\omega_1$ . The open loop transfer function becomes:

$$G(s) = \frac{K_v}{s(\frac{s}{\omega_1} + 1)^2} \quad \text{where } K_v = \frac{K_a K_m K_{vco}}{N} \quad (4)$$

$$|G(s)| = [G(s) \cdot G(-s)]^{1/2}$$

$$|G(j\omega)|_{DB} = +20 \log_{10} K_v - 20 \log_{10} \omega - 10 \log_{10} \left[ \left( \frac{\omega}{\omega_1} \right)^4 + 2 \left( \frac{\omega}{\omega_1} \right)^2 + 1 \right] \quad (5)$$

The phase angle is simply

$$\beta = -\frac{\pi}{2} - 2 \arctan \frac{\omega}{\omega_1} \text{ radians} \quad (6)$$

The phase margin,  $\phi_m$ , is  $\pi$  minus the phase angle.

As indicated by the Nichols chart, a 60 degree phase margin yields 0.5DB peaking in the closed loop response.

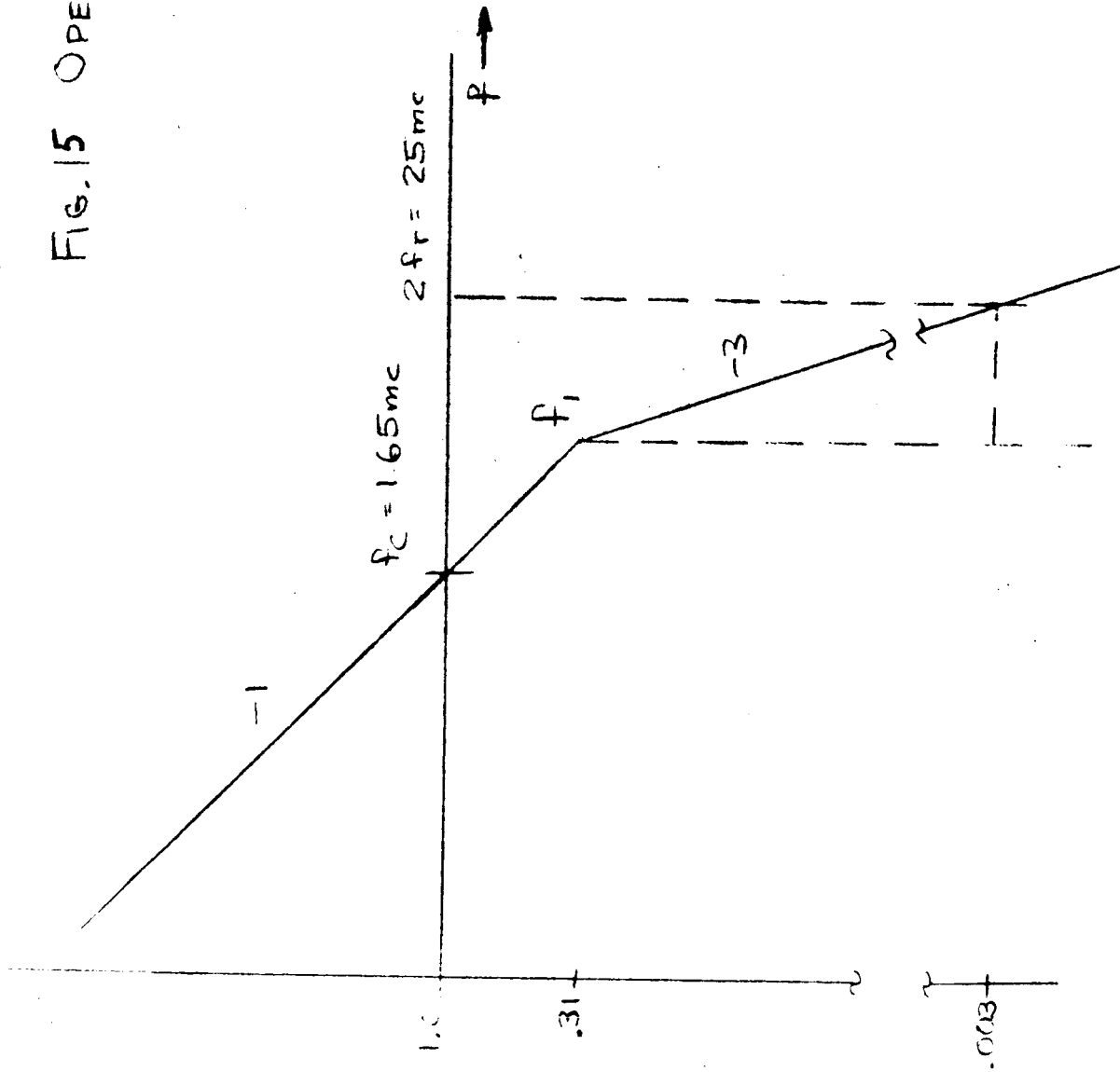
Therefore

$$\phi_m = \frac{\pi}{2} - 2 \arctan \frac{\omega_c}{\omega_1} \quad (7)$$

$$\omega_1 = 3.73 \omega_c \text{ and } \omega_1 = 3.73 K_v \quad (8)$$

The open loop bandwidth was based on the baseband requirements. The open loop gain was determined by the open loop bandwidth and required spurious rejection. Consider Figure 15. The rejection of the 25MC multiplier rejection is established as 50DB below the unmodulated

FIG. 15 OPEN LOOP PARAMETERS



carrier. From the geometry of the figure

$$\omega_c = 33.4 \cdot 10^{+6} \text{ rps} \quad (9)$$

$$\omega_e = 8.98 \cdot 10^{+6} \text{ rps} \quad (10)$$

$$k_v = 8.98 \cdot 10^{+6} \text{ sec}^{-1} \quad (11)$$

The loop parameters were listed as

$$N = 4 \quad (12)$$

$$k_\alpha = 10 \text{ volts/volt} \quad (13)$$

$$k_m = 1 \text{ volts/radian} \quad (14)$$

$$k_{vco} = 3.59 \cdot 10^{+6} \frac{\text{radians}}{\text{volt sec.}} \quad (15)$$

$$\text{and } \frac{\Delta \theta_o}{V_m}(s) = 4.0 \quad (16)$$

The closed loop transfer function is of the form

$$\frac{\Delta \theta_o}{V_m}(s) = \frac{N}{\left(\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n}s + 1\right)\left(\frac{s}{\omega_z} + 1\right)}$$

The parameters  $\xi$ ,  $\omega_n$  and  $\omega_z$  were computed from a real axis plot of the open loop amplitude response.

The closed loop amplitude response was computed as follows:

$$\left| \frac{\Delta \theta}{V_m}(j\omega) \right| = \left[ \frac{\Delta \theta}{V_m}(s) \cdot \frac{\Delta \theta}{V_m}(-s) \right]^{\frac{1}{2}} \quad (17)$$

$$\text{or } \left| \frac{\Delta \theta}{V_m}(j\omega) \right| = 20 \log N - 10 \log \left\{ \left(1 - \frac{2\omega^2}{k_v \omega_n}\right)^2 + \frac{\omega^2}{k_v^2} \left[1 - \left(\frac{\omega}{\omega_z}\right)^2\right]^2 \right\} \quad (18)$$



The amplitude response of equation 18 is listed in Figure 16 and the derivative of the phase response (group delay) is shown in Figure 17. This design yielded the following parameters

Closed loop peaking at 1.5 MC	0.4DB
Rejection at 12.5 MC (Multiplier Feedthru)	-33.8DB
Rejection at 25 MC (Multiplier Sideband)	-50.9DB
Variation in group delay 0 - 500 KC.	5 nanoseconds
Variation in group delay 0 - 1.5 MC	40 nanoseconds.

### (3) Loop Design in the Complex Plane

It was suggested that the previous loop design was far from optimum as the design was based on a 60 degree phase margin. Therefore, the effort was continued and a loop synthesized that exhibited a closed loop response such that the closed loop poles fall on a semicircle in the complex plane. This approach and the results are summarized in the following sections. The root locus plot suggests that if the open loop gain is optimized the closed loop poles can be forced to fall on a semicircle in the left hand plane yielding a Butterworth response. Figure 18 indicates this thought for a third and fourth order Butterworth. The form of the closed loop third order Butterworth response is indicated by equation 19.

$$F_3(s) = \frac{\Delta \theta_o(s)}{N V_m} = \frac{1}{\left(\frac{s}{\omega_n} + 1\right) \left(\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1\right)} \quad (19)$$

The Locked Oscillator Phase Modulator exhibits a pole at the origin in its open loop transfer function. Since the total number of poles must be

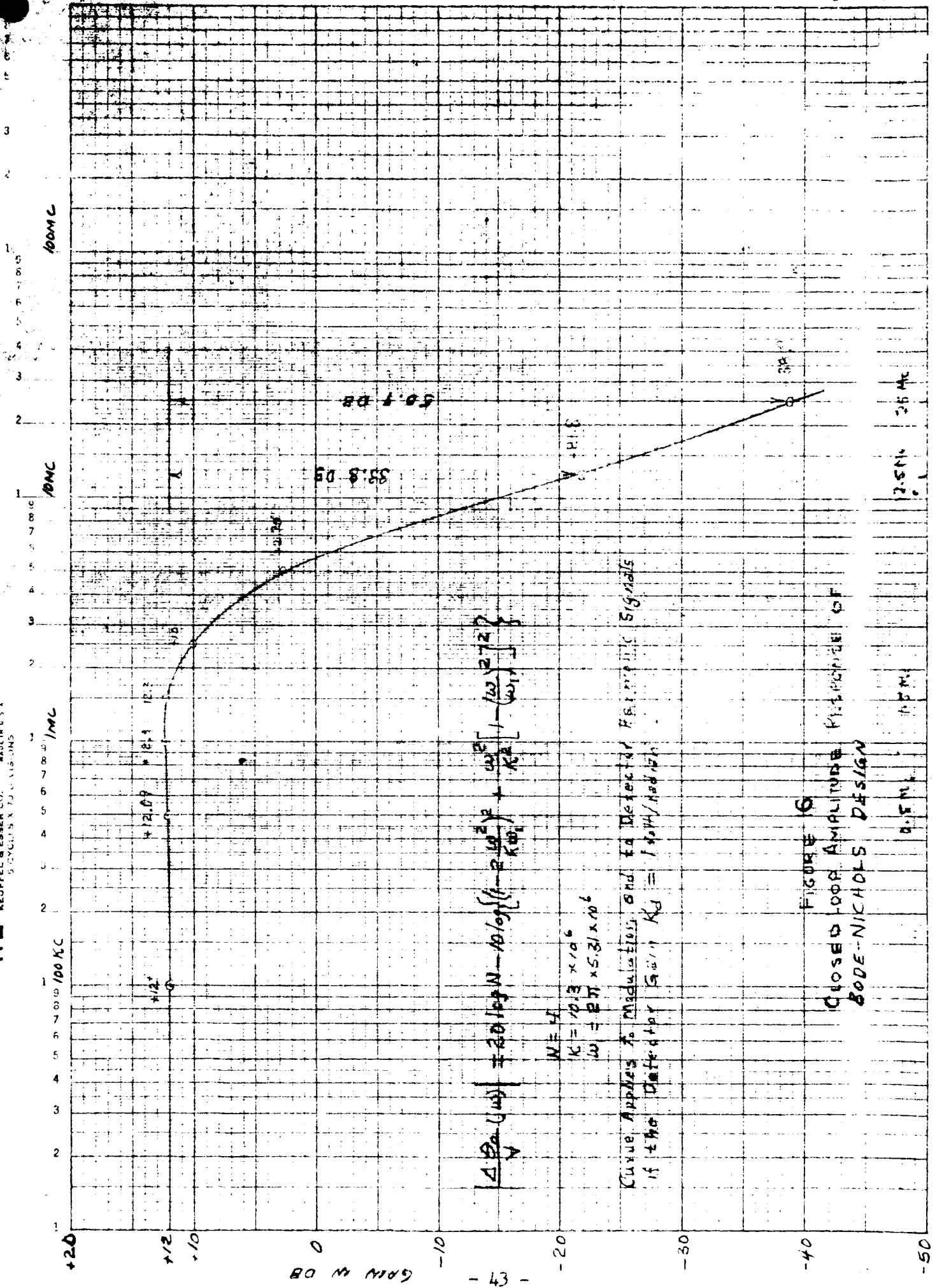


FIGURE 6  
CLOSED-LOOP AMPLITUDE RESPONSE OF  
BODE-NICHOLS DESIGN

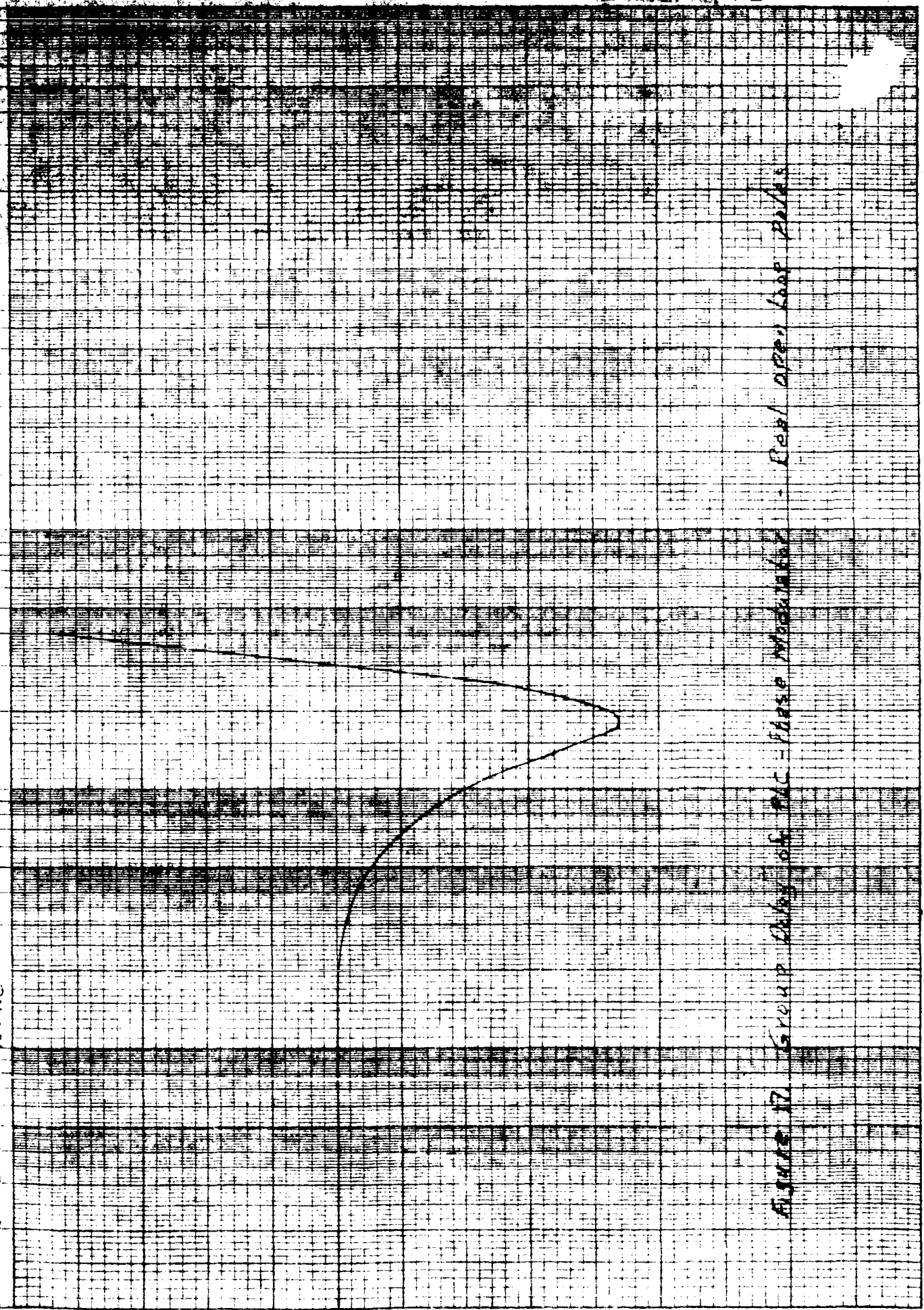
H.E. SEMI-LOGAR. MIC. 10 62'S  
 5 CYCLES X 70 DIVISIONS MIC IN U.S.A.  
 KEUFFEL & ESSER CO.

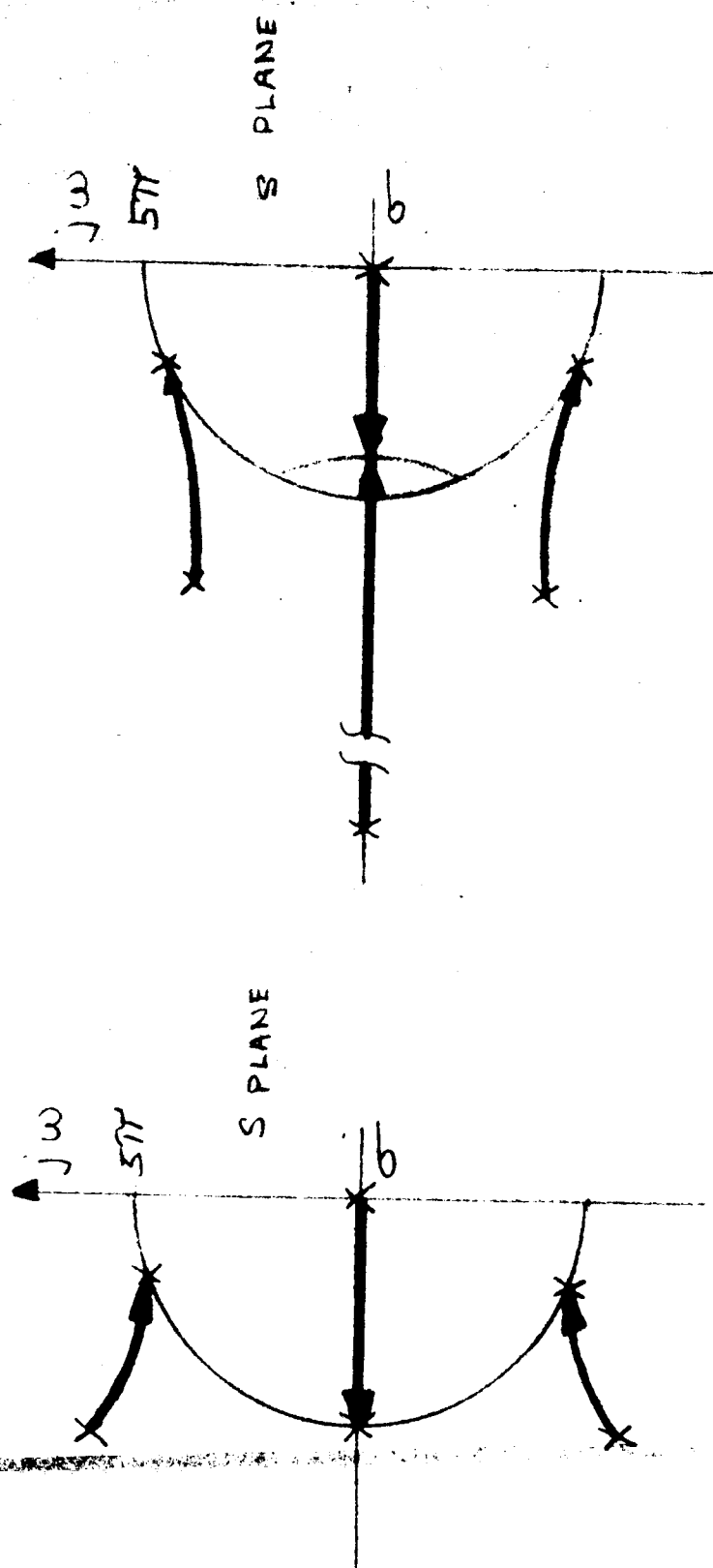
frequency cps 10mc

1000 Kc

SCALE X 10<sup>-7</sup> seconds

Figure 17. Group Delay of MC - Phase Modulator - Real open loop poles





(a) 3rd ORDER SYSTEM (b) 4th ORDER SYSTEM

FIG 18 BUTTERWORTH PHASE-LOCKED  
PHASE MODULATOR - ROOT LOCUS

equal in the open and closed loop functions, we select the open loop transfer function as listed in equation 20.

$$G_3(s) = \frac{K_v}{s \left( \frac{s^2}{\omega_{n0}^2} + \frac{2\epsilon_0}{\omega_{n0}} s + 1 \right)} \quad (20)$$

The closed loop transfer function is written in terms of the open loop parameters by substitution in the familiar relationship

$$F(s) = \frac{G(s)}{1+G(s)} = \frac{1}{\frac{s}{K_v} \left( \frac{s^2}{\omega_{n0}^2} + \frac{2\epsilon_0}{\omega_{n0}} s + 1 \right)} \quad (21)$$

By equating the closed loop relationships described by equation 19 and 21 and solving for open loop parameters we may synthesize a closed loop transfer function having a Butterworth characteristic. The equality is listed in equation (22)

$$\frac{s^3}{K_v \omega_{n0}^2} + \frac{2\epsilon_0}{\omega_{n0}} s^2 + \frac{s}{K_v} + 1 = \frac{s^3}{\omega_n^3} + \frac{2\epsilon+1}{\omega_n^2} s^2 + \frac{2\epsilon+1}{\omega_n} s + 1 \quad (22)$$

The parameters of interest become

$$K_v = \frac{\omega_n}{2\epsilon+1} \quad (23)$$

$$\omega_{n0} = \omega_n \sqrt{2\epsilon+1} \quad (24)$$

$$\epsilon_0 = \frac{\omega_{n0}}{2\omega_n} \quad (25)$$

For a third order Butterworth  $\xi$  is 0.5. The remaining parameters are determined as a function of  $\omega_n$ .  $\omega_n$  was determined by examining published curves ("Reference Data for Radio Engineers", 4th Edition, chap. 7, page 194) and determining the value of  $\omega_n$  for a third order Butterworth such that the amplitude droop is 0.2DB at 1.5MC. The following parameter values follow:

$$\omega_n = 5\pi \cdot 10^6 \text{ rps} \quad (26)$$

$$K_v = 2.5 \pi \cdot 10^6 \text{ sec}^{-1} \quad (27)$$

$$\omega_{n0} = \sqrt{2} \ 5 \pi \cdot 10^6 \text{ rps} \quad (28)$$

$$\xi_0 = 0.707$$

The open loop transfer function becomes

$$G_3(s) = \frac{2.5 \pi \cdot 10^6}{s \left( \frac{s^2}{50 \pi^2 \cdot 10^{+12}} + \frac{s}{10 \pi \cdot 10^6} + 1 \right)}$$

The open and closed loop amplitude response and group delay of both a third order and fourth order Butterworth are listed in Figures 19 thru 22.

The same technique was applied to synthesize additional closed loop responses that exhibit a three pole and four pole Bessel response (Linear Phase Response). The root locus is shown in Figure 23.

The closed loop amplitude and group delay for the three and four pole Bessel is shown in Figures 24 thru 27. Table VII indicates a summary of the parameters of the various loop designs.

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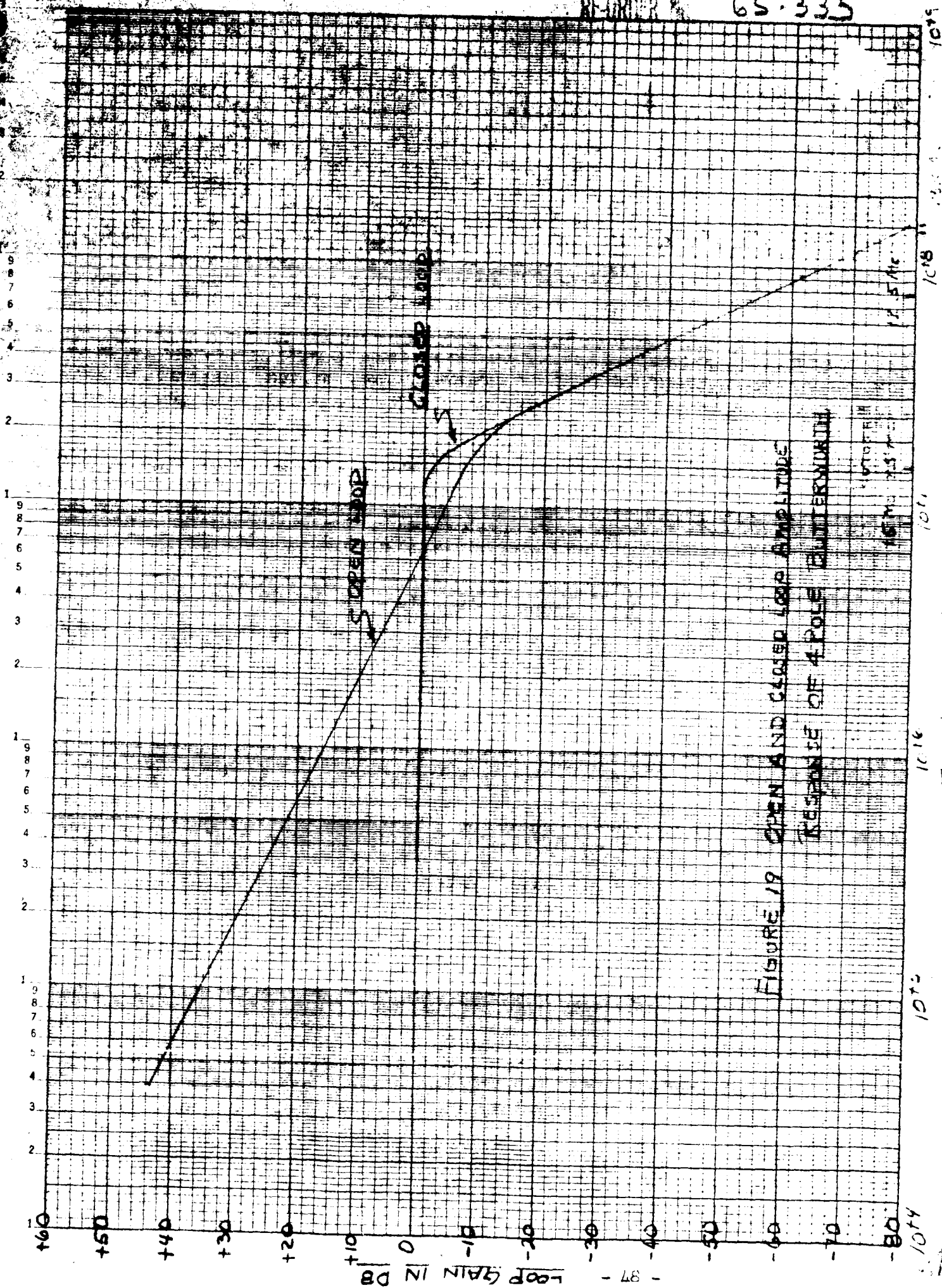


FIGURE 19 OPEN AND CLOSED LOOP AMPLITUDE RESPONSE OF 4 POLE BUTTERWORTH

10<sup>4</sup> 10<sup>5</sup> 10<sup>6</sup> 10<sup>7</sup>



NEUFELD & ASSOCIATES, INC. MADE IN U.S.A.  
5 CYCLES X 70 DIVISIONS

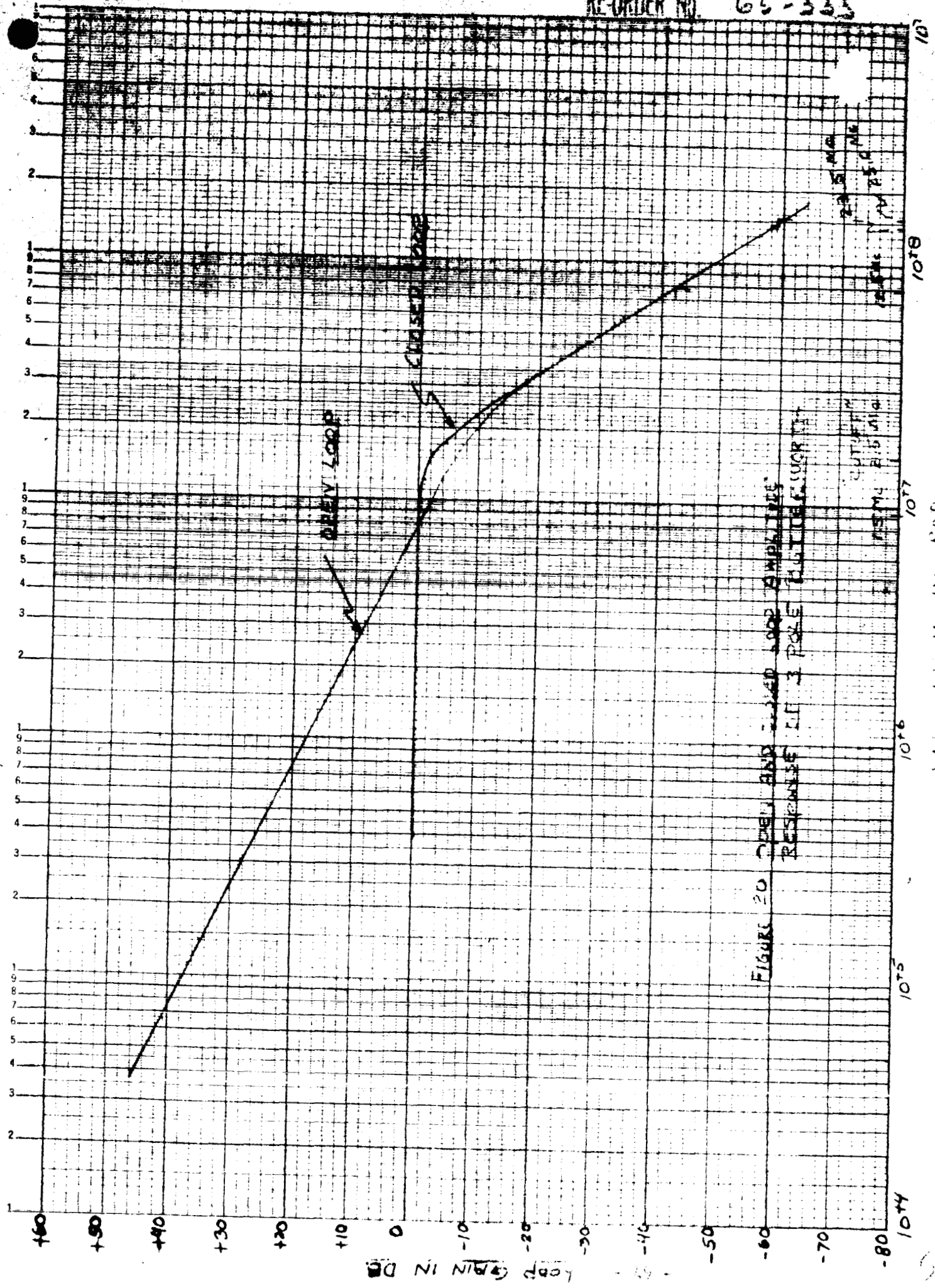


FIGURE 20 OPEN AND CLOSED LOOP AMPLIFIERS  
RESPONSE IN 3 POLE MULTISTAGE CIRCUIT

100 V IN RAD/SEC



K&E SEMILOGARITHMIC 40 0213  
 5 CYCLES X 70 DIVISIONS MADE IN U.S.A.  
 K&E SEMILOGARITHMIC 46 0213  
 5 CYCLES X 70 DIVISIONS MADE IN U.S.A.  
 KUPPEL & ESSER CO

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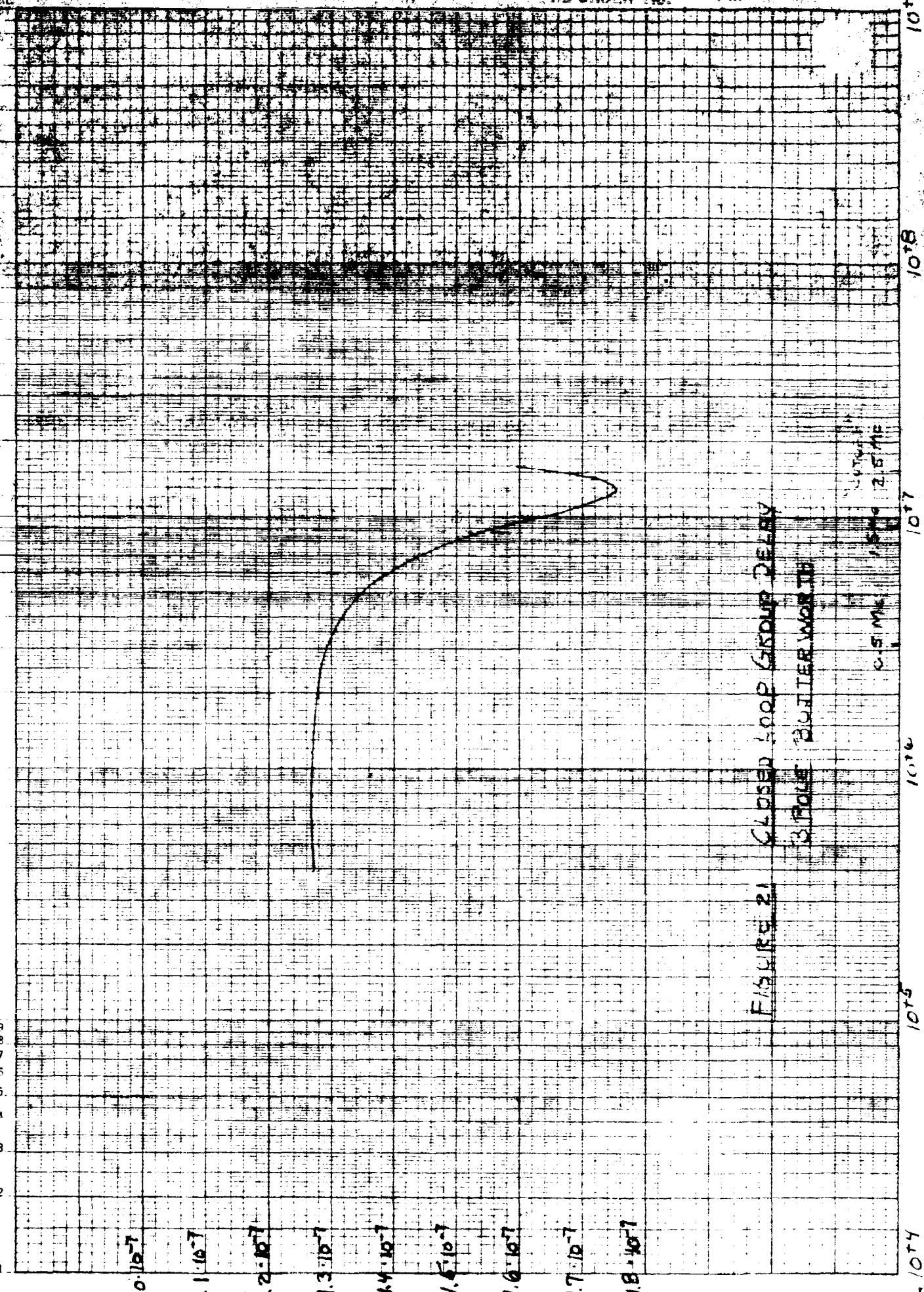


FIGURE 21 CLOSED LOOP GROUP DELAY  
 3 POLE BUTTERWORTH

0.5 MHz  
 1.5 MHz  
 2.5 MHz

GROUP DELAY IN SEC.

FREQUENCY IN HZ.

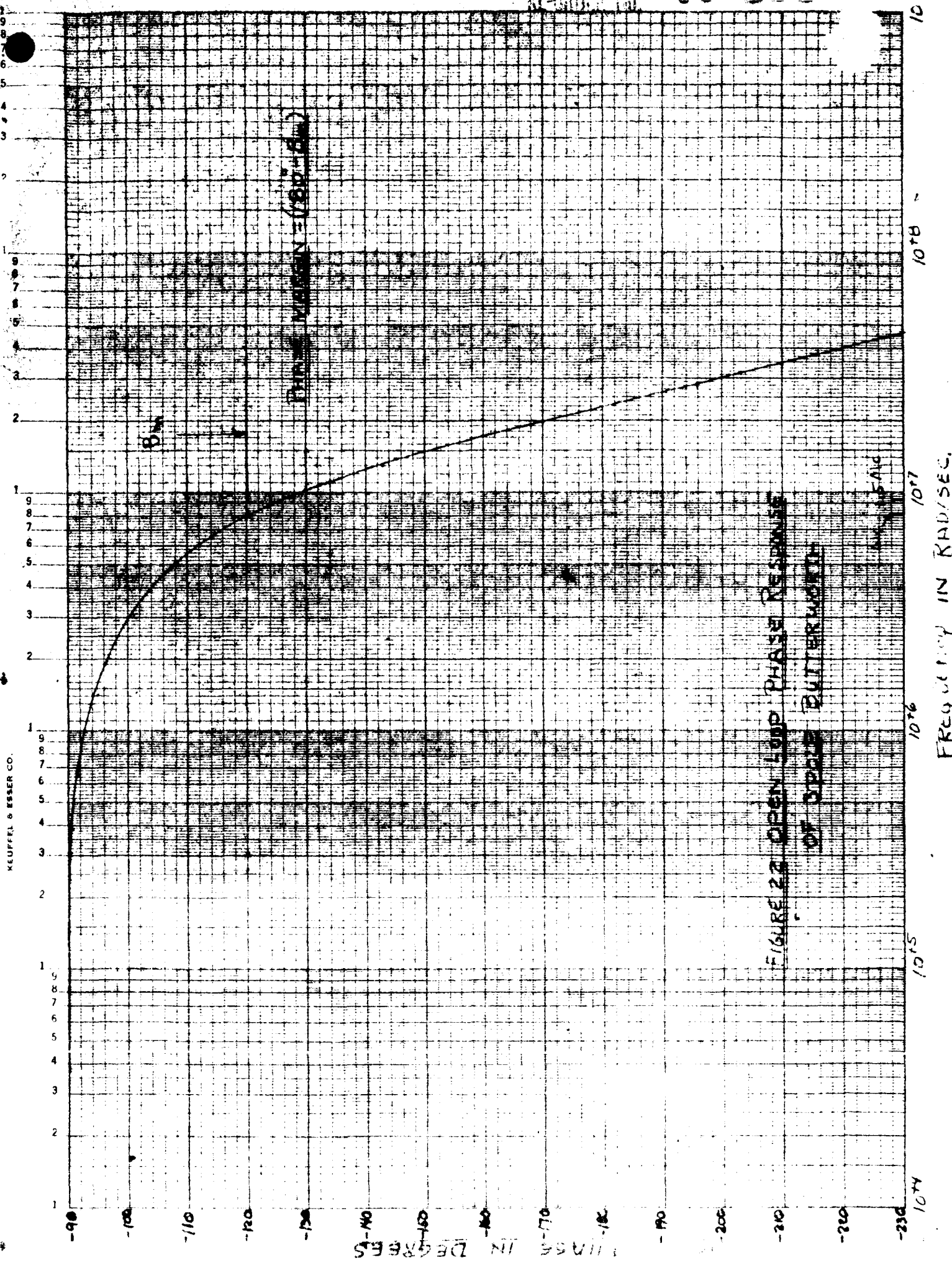
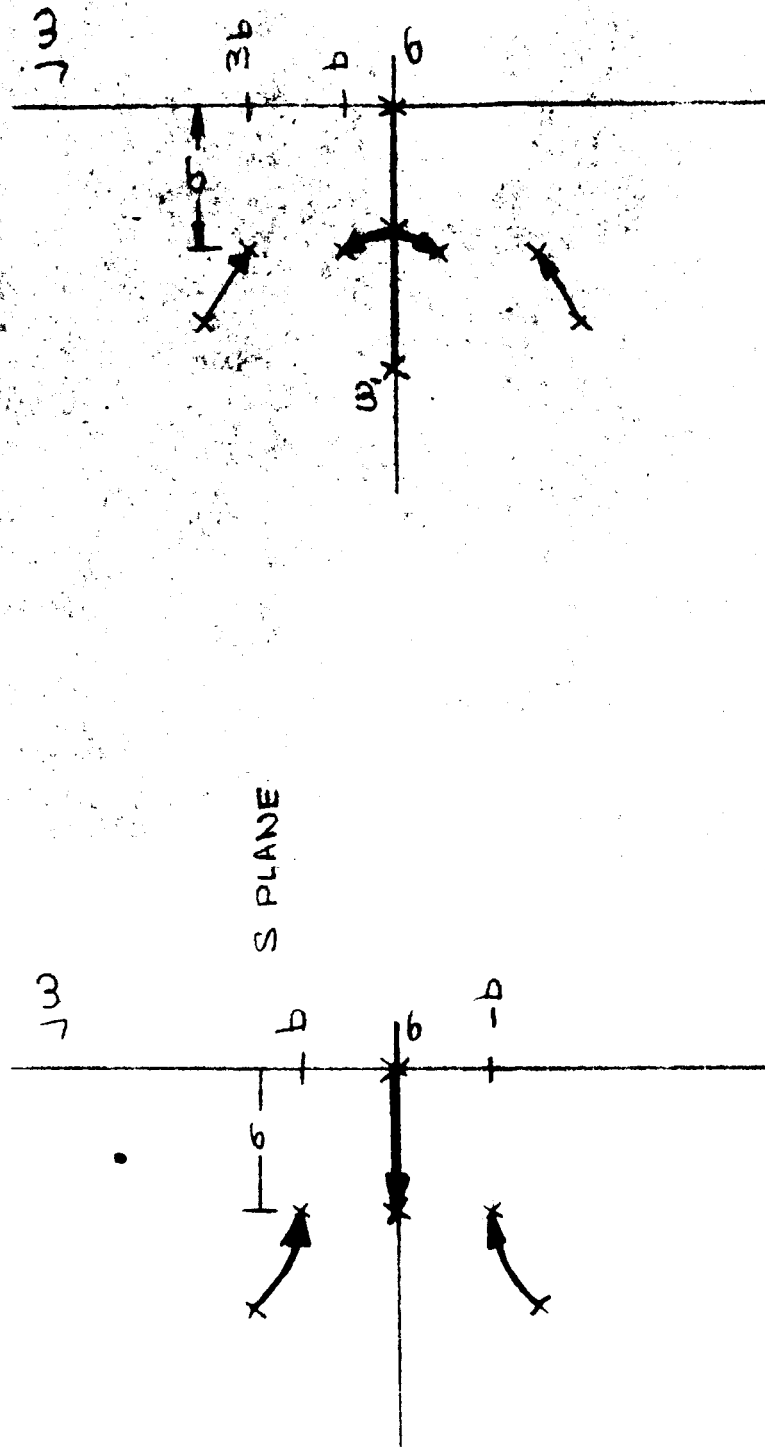


FIGURE 22 OPEN LOOP PHASE RESPONSE  
 OF BUTTERWORTH



(a) 3 POLE APPROXIMATION (b) 4 POLE APPROXIMATION

FIGURE 23 CONSTANT DELAY PHASE LOCK  
PHASE MODULATOR APPROXIMATION - ROOT LOCUS

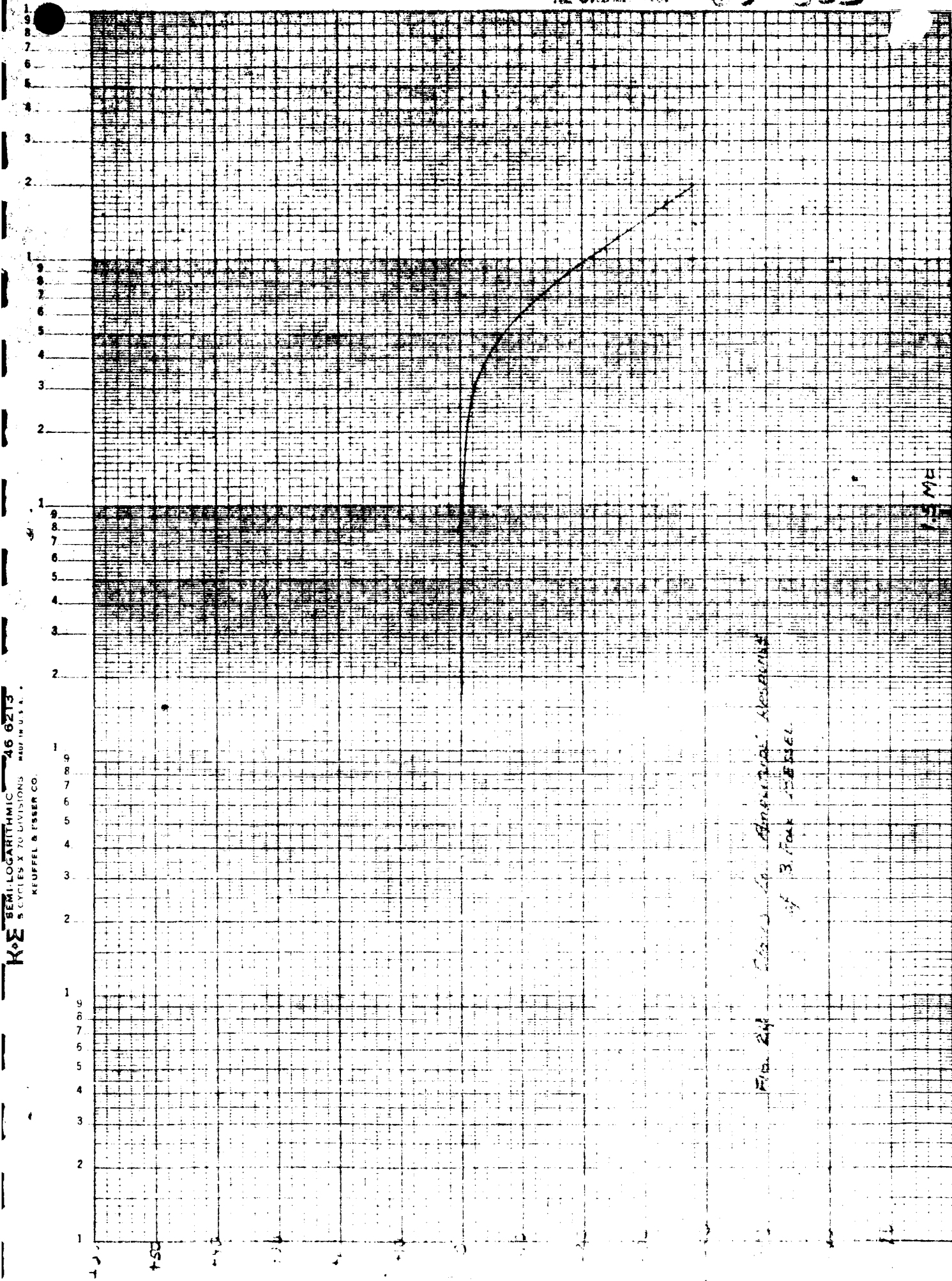


Fig. 24  
of 3 FOR SERIES

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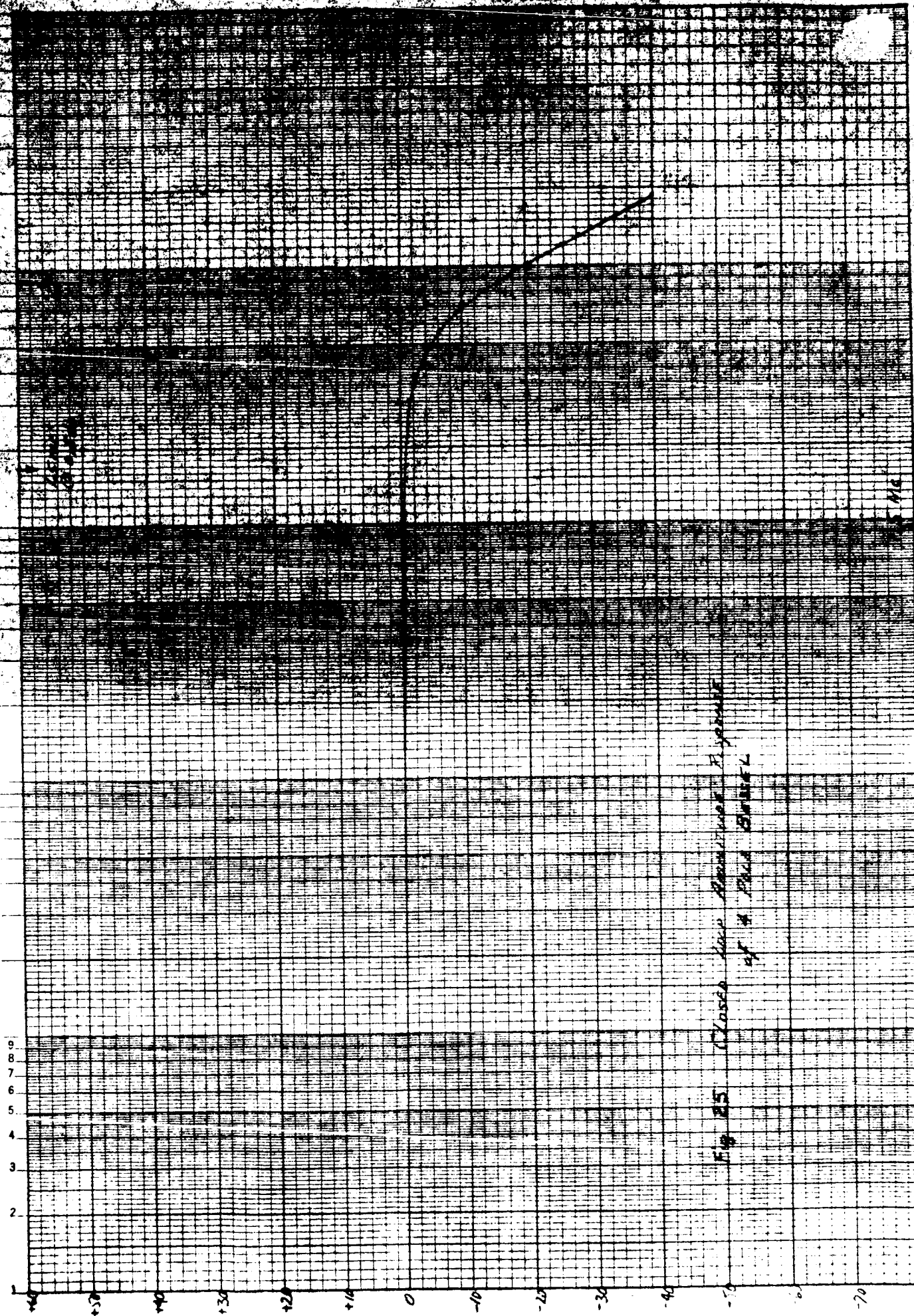


Fig. 25 Closed Loop Amplifier Frequency  
 of a Pilot Amplifier

FREQUENCY (RAD/SEC)

- 95 - LOSS GAIN IN DB



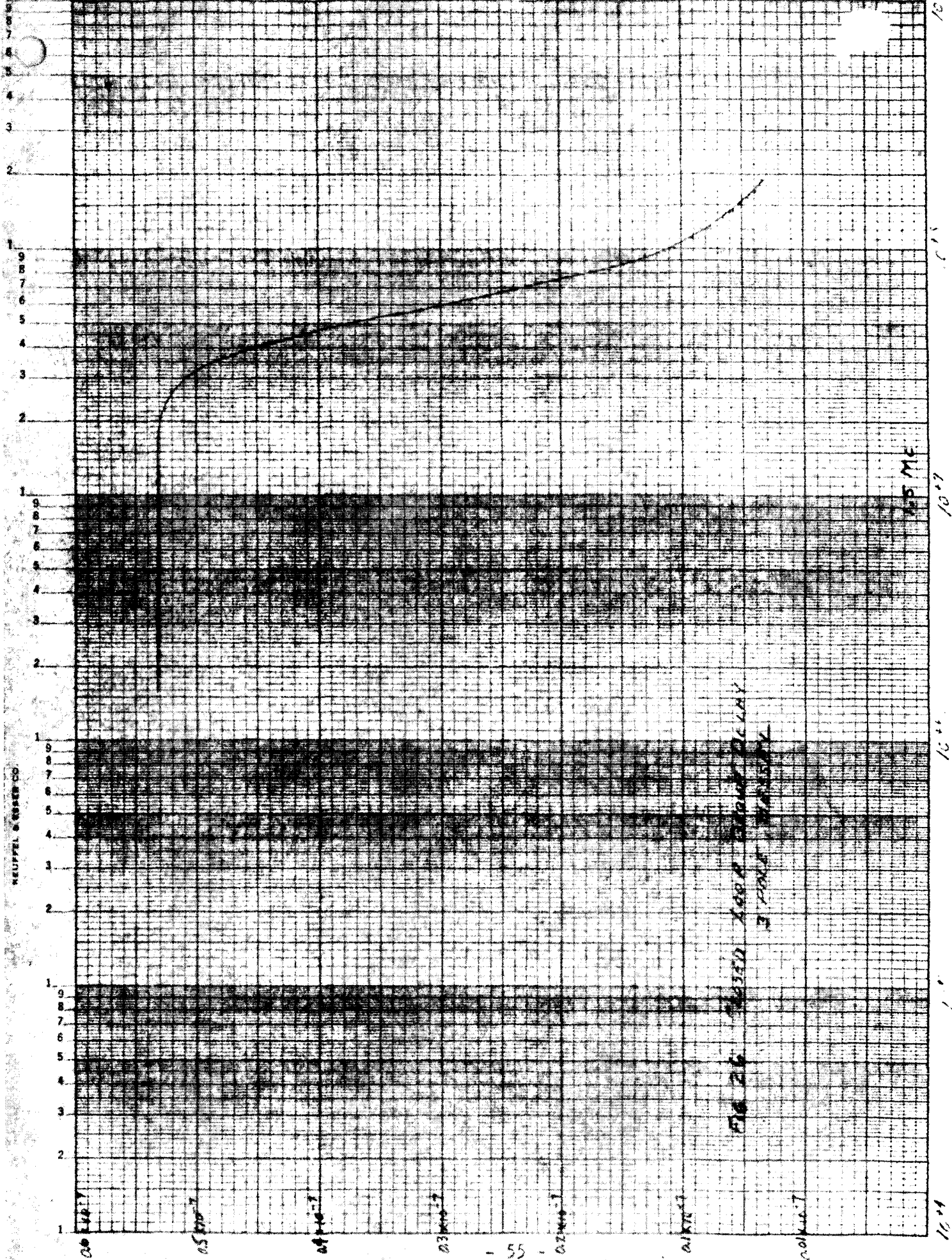


FIG. 26. GROUP DELAY IN SEC. vs. FREQUENCY IN RAD/SEC. for a 3 pole network

68

RE-0207 64-235

K-2 SEMI-LOGARITHMIC  
% CYCLES X 70 DIVISIONS MADE IN U.S.A.  
KEUFFEL & ESSER CO.

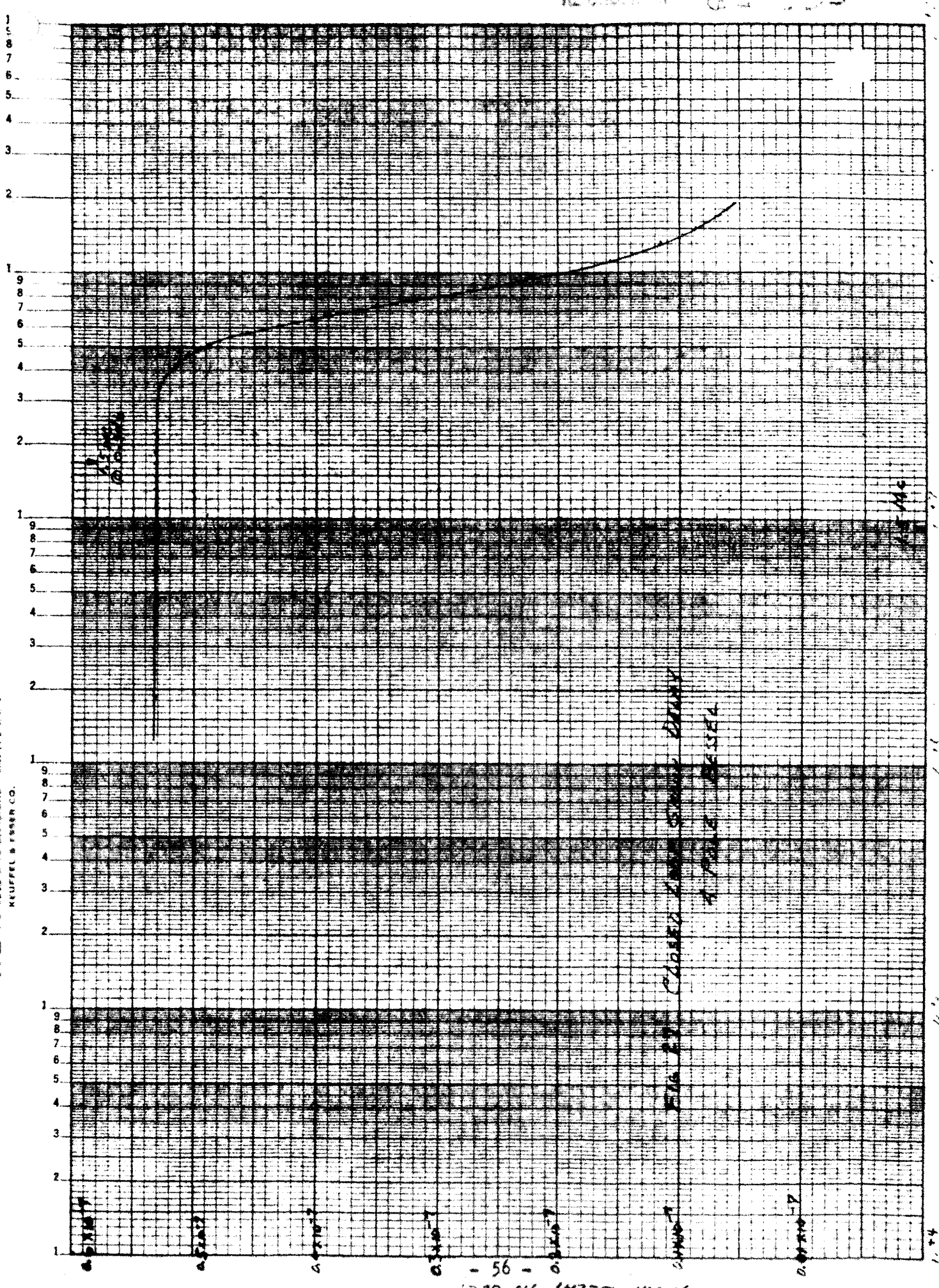


FIG. 2. CLOSER TO THE SOURCE DELAY  
A. 100.0 MILES

FREQUENCY (KAL/SEC)

GROUP DELAY IN SEC

59

Loop Design	Phase Margin	Butterworth		Bessel	
		3rd Order	4th Order	3rd Order	4th Order
125 MC Rejection	-33.8DB	-42DB	-56DB	-13DB	-13DB
25 MC Rejection	-50.9DB	-60DB	-78DB	-31DB	-34DB
Amplitude Response to 1.5 MC	0.2DB	0.2DB	0.2DB	0.2DB	0.2DB
Variation in Group Delay to 1.5 MC	$40.10^{-9}$ sec	$38.10^{-9}$ sec	$47.10^{-9}$ sec	$4.010^{-9}$ sec	$4.010^{-9}$ sec

Table VII Summary of Design Characteristics

(4) Evaluations and Recommendations

It is clear that high fidelity angular modulation systems require constant group delay vs frequency characteristics to avoid intermodulation of an ensemble of signals, thus the fourth order Bessel distribution is preferred. However, the out of band rejection becomes -30.5DB and -51.5DB, respectively and the group delay remains essentially less than one nanosecond. Assuming that the phase detector reference is 12.5 mc and the phase detector balance is designed to yield an additional 20DB rejection of the 12.5 mc feedthrough then the spurious rejection of the 4 pole Bessel is adequate and the group delay variation superior.

d. Practical Problems in Mechanization

(1) Feedback Divider

The specification demands that the peak phase deviation be  $\pm 4$  radians-obviously beyond the range of realizable phase detectors. Thus the feedback divider is required to compress the phase deviation.



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At first thought, one may increase  $N$  from 4 to some larger value thus relieving the phase detector linearity requirements. However, the baseband is not compressed by increasing  $N$ , further the phase detector harmonic frequencies and the baseband converge as  $N$  is increased and the loop rejection requirements become intolerable.

## (2) Linearity Considerations

The linearity of the components within the loop is important in satisfying the required fidelity spec. However, one of the primary purposes of feedback is to improve linearity. The improvement is dependent on the location of the non linearity within the loop. The principal sources of non linearity within the phase locked phase modulator are the VCO and Phase Detector. The non linearity problem of the Phase Locked Modulator is more difficult than the usual system is that two principal non linearities are cascaded with the loop. The approach considered in Appendix D is to consider the intermodulation contributions of the phase detector non linearities independently in the open loop condition. The same approach is applied to the VCO. The computations show that the phase detector introduces odd order spectra other than the desired components while the VCO introduces even order undesired spectra. It is assumed that the intermodulation components generated within the phase detector and VCO as a result of the specified two tone test are not additive.

To aid in interpreting the affect of the feedback loop in compensating for the component non-linearities, the quasi-linear model of figure 28 is assumed. The intermodulation sources are assumed to be

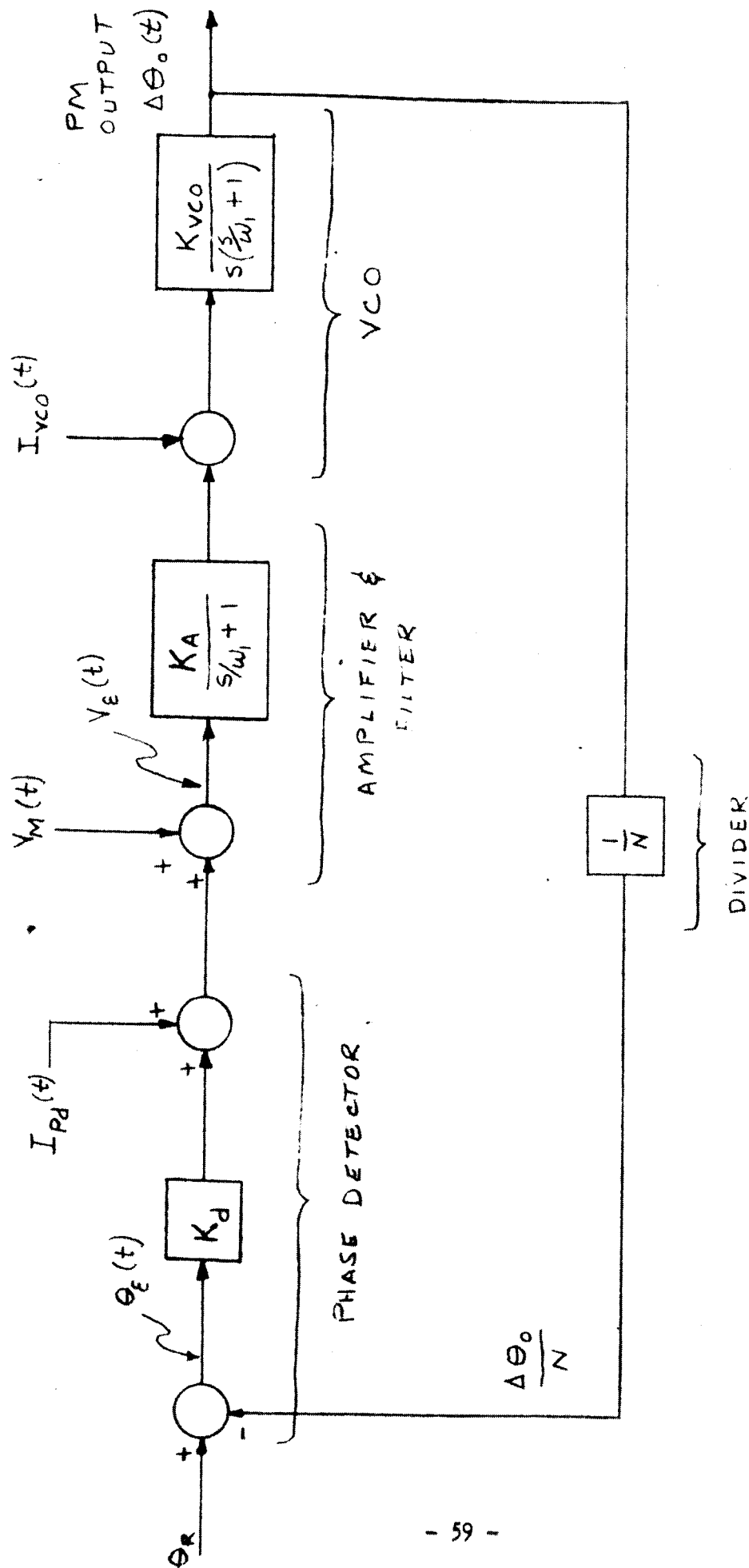


FIG 28 Quasi-Linear Phase Modulator Loop With Intermodulation Sources (Diagram based on Bode-Nichols example)

voltages added to the forward channel at the output of the phase detector and the input to the VCO.

(a) Effect of Loop on VCO Nonlinearity

From the model of figure 24 the error voltage  $V_E(s)$  (at the system null point) as a function of the VCO non linearity is:

$$\frac{V_E(s)}{I_{VCO}(s)} = \frac{\frac{K_{VCO} K_m}{Ns (\frac{s}{\omega_1} + 1)}}{1 + \frac{K_V}{S (\frac{s}{\omega_1} + 1)^2}} = \frac{1}{K_\gamma} \frac{(\frac{s}{\omega_1} + 1)}{(\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n} s + 1)(\frac{s}{\omega_1} + 1)} \quad (29)$$

or 
$$V_E(s) = 1/K_\gamma \quad (30)$$

In the detail computations of Appendix D it was shown that a VCO with 1% non linearity and  $\pm 4$  radians phase deviation driven by a loop amplifier with  $K_\gamma = 3.16$ , the resulting maximum even order intermodulation is -44DB with respect to the unmodulated carrier. Therefore, an amplifier scale factor of  $K_\gamma$  equal to 10 is assumed to further attenuate the affects of VCO non-linearity.

(b) Effect of Loop on Phase Detector Non-Linearity

By a similar analysis the estimate of the phase detector odd order intermodulation source  $I_{PD}(s)$  is expressed as:

$$\frac{V_E(s)}{I_{PD}(s)} = \frac{1}{1 + \frac{K_V}{S (\frac{s}{\omega_1} + 1)^2}} \quad (31)$$

$$\frac{V_E(s)}{I_{PD}(s)} = \frac{1}{K_V} \frac{s\left(\frac{s}{\omega_1} + 1\right)^2}{\left(\frac{s^2}{\omega_n^2} + \frac{2\xi s}{\omega_n} + 1\right)\left(\frac{s}{\omega_2} + 1\right)} \quad (32)$$

From equation 32, the loop's influence on the phase detector non-linearity is frequency sensitive. At high frequencies ( $\omega > \omega_c$ ) the loop performs virtually no correction of the phase detectors non-linearities. Therefore, detailed computations were performed in Appendix D to relate phase detector intermodulation (spurious to unmodulated carrier) as a function of phase detector linearity and excursion. Initially, a sinusoidal phase detector was considered with  $\pm 4$  radian deviation and  $\pm 1$  radian deviation. Further, a phase detector with a sawtooth transfer of  $\frac{E_o}{\theta_{1\omega}}$  (ideally linear to  $\pm \pi$  radians) with 1%, 5% and 10% non linearity over the  $\pm \pi$  range was considered. The input phase deviation was constrained to  $\pm 1$  radian. The details of this investigation are included in Appendix D. However, a sawtooth phase detector, with a dynamic range of  $\pm \pi$  radians and 5% non linearity with the phase deviation of the input constrained to  $\pm 1$  radian yielded spurious -60DB with respect to the unmodulated carrier.

#### e. Implementation of Circuits

Appendix D includes an investigation of each circuit component included in the Locked Oscillator Phase Modulator. Refer to section IV of Appendix D for this discussion.

#### 2. Deviation Multiplication Phase Modulator

As an alternative to the locked oscillator phase modulator, a

brief investigation was made to evaluate the feasibility and comparative advantages that might exist by utilizing conventional phase modulator and deviation multiplication techniques. The details of this investigation are included in Appendix E. The following is a summary of Appendix E.

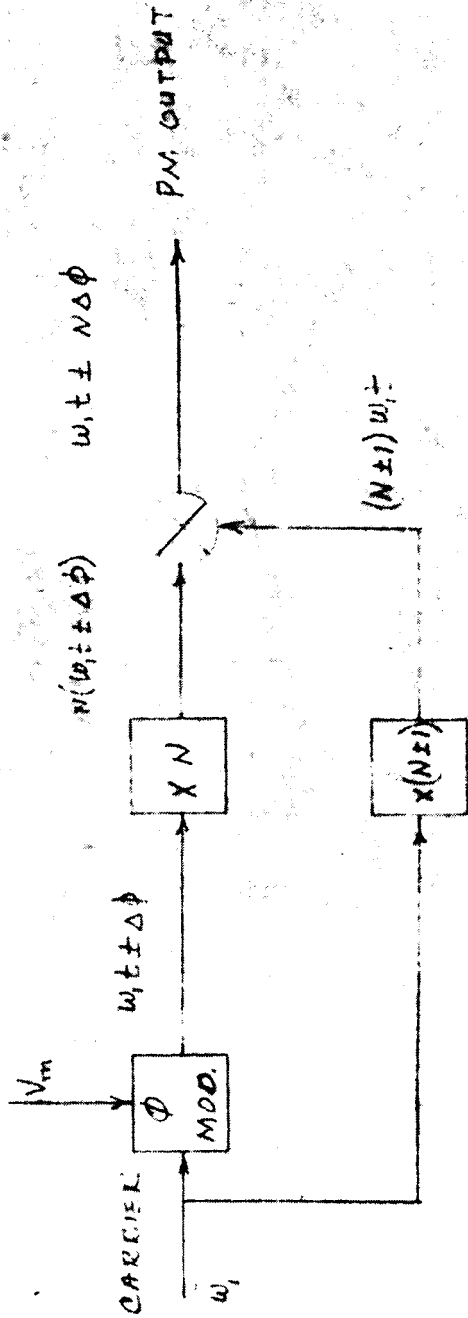
Examination of the basic modulator (assuming an Armstrong type) indicated that for the fidelity (linearity of modulation) required by the RF Test Console, the realizable deviation must be limited to approximately  $1/8$  radian. Therefore the required peak deviation of 4.0 radians necessitates frequency multiplication by at least a factor of 32 within the transmitter in order to maintain intermodulation components at levels of at least -40 db relative to the modulated carrier.

The mechanization of a small deviation frequency multiplication FM transmitter may follow the dual mixer multiplier of Figure 29a (or the direct single mixer of Figure 29b) or the direct multiplier single mixer of Figure 30a. With the necessary amplifiers and filters the circuit implementations are as shown in Figures 29b and 30b. In the direct multiplier chain of Figure 30b a multiplier factor of  $N = 36$  was used to ease the design of the reference channel since the numbers 31 and 33 do not permit cascading of small frequency multiplications.

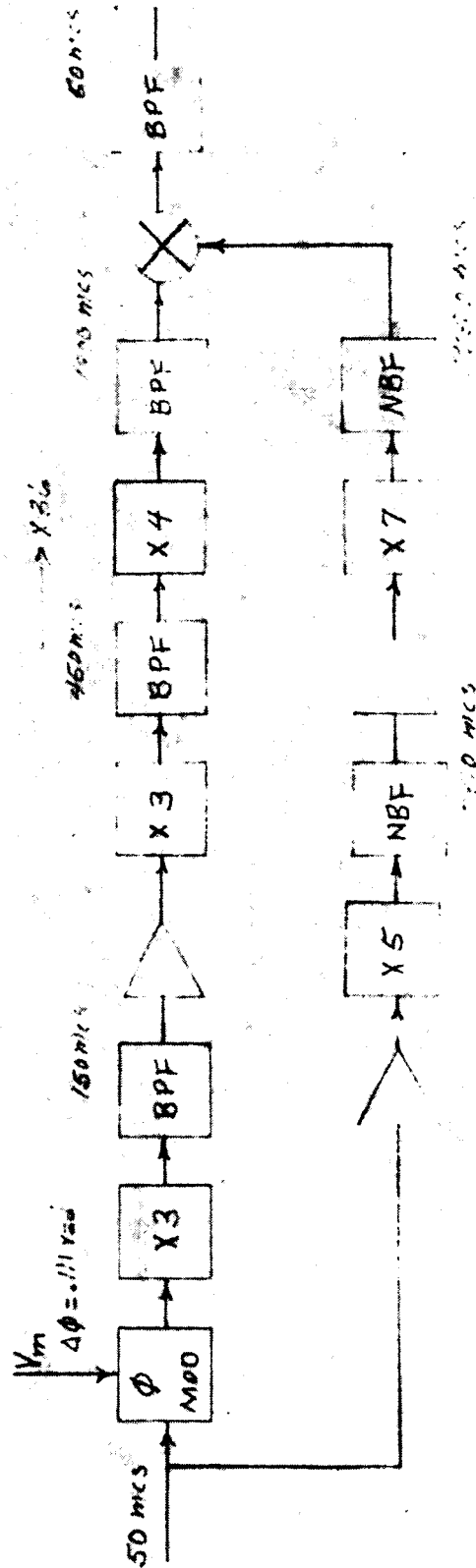
Of these two systems the configuration of Figure 30b is slightly less complex and is not as susceptible to spurious and undesired cross-products caused either by leakage or by heterodyne mixing. In addition to the general problems of amplification, (which is necessary for isolation and for sufficient drive to the multipliers and mixers)

FIG. 29 DUNE HILL, N. H.

FIG. 29 DUNE HILL, N. H.



(a) General modulation



(b) Frequency division by N

FIG 20 Error in Frequency Division by N

and frequency multiplication, a severe problem exists in either circuit in the design and fabrication of Bessel filters in the modulation channels. The direct multiplier chain requires 4 such filters; the dual-mixer multiplier, 5. In either instance the composite bandwidth characteristic of the filters, all in cascade, must provide (in instance) a flat delay (linear phase) response over an absolute modulation bandwidth of at least 9 mcs.

Examination of the complementary RF Test Console mode of operation using frequency modulation at a deviation of 500 kc and with modulation frequencies extending to approximately dc, say 3 cps, shows a requirement for a peak deviation of  $1.67 \times 10^5$  radians. These PM systems are inadequate for dual mode PM/FM operation under these conditions without extensive additional effective multiplication.

Considerations of performance, design time, circuit complexity, ease of mechanization and modification, economy, and dual mode PM/FM utilization of deviation multiplication modulators as compared to the same factors for the locked oscillator modulator indicate that the latter is preferable for the RF Test Console.



### 3. P. M. Receiver

Appendix F of this report contains the details of the P.M. Receiver study. The following constitutes a summary of that effort.

#### a. PM Receiver Block Diagram

The portion of the statement of work pertaining to the PM receiver is summarized as follows: Perform an analysis of the PM Receiver which satisfies the requirements of JPL Spec. GPG-15062-DSN par. 3.5.1. The analysis shall include the tracking loop design and an investigation of the achievable dynamic range of the demodulator wideband phase detector. The analysis shall yield a block diagram indicating impedance levels and the dynamic range of signal and noise voltages. Concentrate the P.M. receiver experimentation on the wide-band phase detector, the tracking loop and input amplifier to the extent sufficient to support a valid PM receiver design plan during a later implementation phase.

Figure 1 includes the PM Receiver block diagram. The receiver configuration is essentially the same as outlined in the JPL specification with the following exceptions: 1) The 60 MC VCO is mechanized as a 1 MC precision VCO and X60 frequency multiplier 2) The 10 MC reference oscillator is mechanized as a precision 1 MC oscillator and X10 frequency multiplier 3) An additional 100 KC noise

bandwidth filter is provided such that the receiver bandwidth at 50 MC can be changed from 10 MC to 100 KC thus enabling the tracking loop to be tested at threshold in a 2 BLO of 3.0 cps without noise overloading the receiver front end. 4) A precision variable attenuator is provided at the receiver input to constrain the required AGC dynamic range for the 100dB S/N dynamic range. 5) The predetection record system is mechanized with an additional stage of up and down conversion to allow the full 6 MC information spectrum to be centered on a 5 MC center frequency without spectrum foldover. 6) The predetection playback system has been altered to include a stage of up conversion to prevent second harmonic components of the playback information from feeding thru the 10 MC IF amplifier.

b. Tracking Loop Signal and Noise Power Levels

Figure 31 indicates signal and noise power levels and S/N matrices referenced to noise bandwidths of 10 MC, 6 MC, 2 KC and 3 cps. These bandwidths are referenced as they constitute the noise bandwidths of the receiver front end, demodulation channel, tracking loop predetection bandwidth and the minimum tracking loop bandwidth. Figure 32 indicates the noise and signal power levels from the receiver front end thru the tracking loop for maximum and minimum S/N ratios. Further, the gain (or loss) and linear power capability of each unit from the receiver front end thru the tracking loop is shown.

c. Demodulation Channel Signal and Noise Power Levels

Figure 33 indicates the same data from the receiver front end thru the demodulation channel. Without dwelling on the detail outlined

98

12.3.6. 6.4.3.25

COLUMN

	1	2	3	4	5	6
S	-20	-20	-40	-50	-60	-70
N	-70	+50	+40	+20	+10	0
1						
2						
3						
4						
5						
6						

dBm

(A) NOISE BW = 3.6 Hz

COLUMN

	1	2	3	4	5	6
S	-20	-20	-40	-50	-60	-70
N	-70	+50	+40	+20	+10	0
1						
2						
3						
4						
5						
6						

dBm

(B) NOISE BW = 3.6 Hz

COLUMN

	1	2	3	4	5	6
S	-20	-30	-40	-50	-60	-70
N	-70	-23	-33	-43	-53	-63
1						
2						
3						
4						
5						
6						

dBm

(C) NOISE BW = 6 Mc

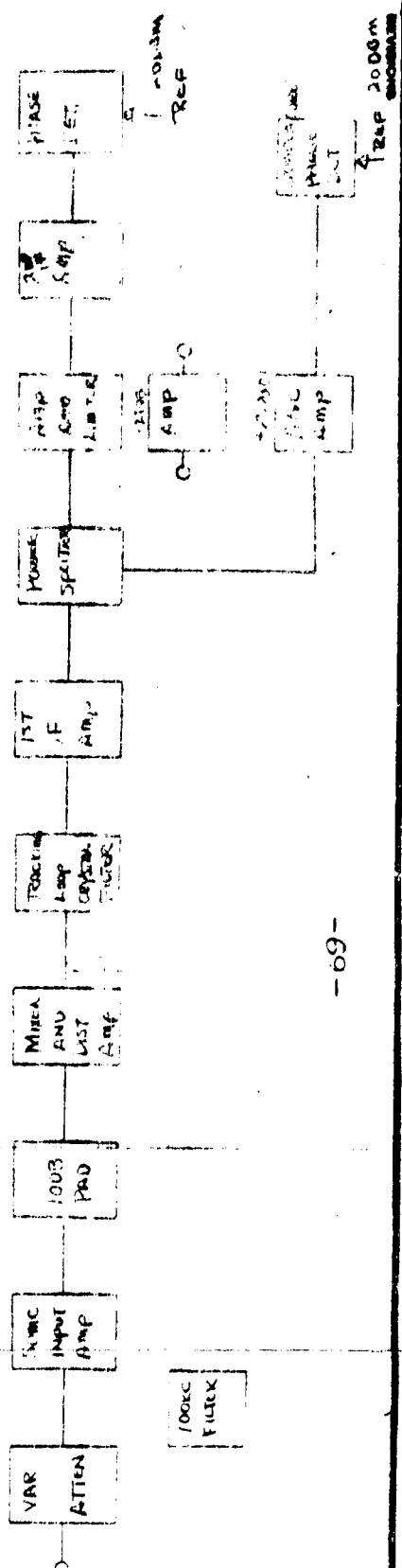
COLUMN

	1	2	3	4	5	6
S	-20	-20	-40	-50	-60	-70
N	-70	-23	-33	-43	-53	-63
1						
2						
3						
4						
5						
6						

dBm

(D) NOISE BW = 1 Mc

FIGURE 31 S/N RATIO AS A FUNCTION OF NOISE BANDWIDTH

[illegible]

## CONCLUSIONS

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in Appendix F, the following portions of the receiver design plan are essential 1) The demodulation channel phase detector (predetection noise bandwidth of 6 MC) will operate at a minimum S/N ratio of -40DB. The phase detector S curve will be linear to 40 volts peak to peak 2) The tracking loop predetection S/N ratio will be -28.24DB at threshold with a 2BLO of 3.0 cps. 3) The linear power capability of each unit in the receiver must be larger than usual as the simulated noise levels at the receiver input are higher than would be normally experienced. 4) The demodulation channel predetection bandwidth is established by a Bessel filter. The predetection gain is achieved by wideband gain and phase stable amplifiers. 5) The Input amplifier gain is attributed to wideband gain and phase stable feedback amplifiers. The bandwidth is established by a linear phase filter. 6) The gain of the Input amplifier is changed as a function of AGC by changing the insertion loss of interspace voltage sensitive attenuators.

d. Carrier Tracking Loop Design

The carrier tracking loop predetection bandwidth is established by a crystal filter with a 2 KC noise bandwidth centered on 10MC. The predetection gain is attributed to gain and phase stable broadband feedback amplifiers.

The tracking filter components were computed for predetection noise bandwidths of 3, 12, 20 and 48 cps. The tracking loop filter design was based on the JPL design as outlined by Rechtin and Jaffe and summarized as follows:

Threshold Loop Gain:  $G_o = \alpha_o G$  (33)

Threshold Limiter Suppression Factor:  $\alpha_o$  (34)

Loop Filter Transfer Function:  $F_1(s) = \frac{1 + \tau_2 s}{\tau_1 s}$  (35)

Threshold Loop Noise Bandwidth:  $2 B_{Lo} (\text{cps}) = \frac{3}{2\sqrt{2}} B_o (\text{rps})$  (36)

Filter Time Constants:  $\tau_2 = \frac{\sqrt{2}}{B_o}$   $\tau_1 = \frac{G_o}{B_o^2}$  (37)

Open Loop Transfer Function:  $H_o(s) = \frac{G_o}{s} F_1(s) = \frac{B_o^2 (1 + \frac{\sqrt{2}}{B_o} s)}{s^2}$  (38)

Closed Loop Transfer Function:  $H(s) = \frac{1 + \frac{\sqrt{2}}{B_o} s}{\frac{s^2}{B_o^2} + \frac{\sqrt{2}}{B_o} s + 1} = \frac{1 + \frac{3}{4B_{Lo}} s}{\frac{9s^2}{32B_{Lo}} + \frac{3}{4B_{Lo}} s + 1}$  (39)

The no noise loop gain ( $G$ ) was made sufficient to constrain the static phase error to one degree when the transmitter standard is detuned 500 cps ( $G = 180,000$ ). The limiter suppression factor  $\alpha_o$  is 0.02 for the minimum predetection signal to noise ratio of -28,24 DB. It follows that the threshold loop gain,  $G_o$ , is 3600. The filter time constants were computed and listed in Appendix F for a threshold loop gain of 3600 and predetection noise bandwidths of 3.0, 12.0, 20.0 and 48.0 cps. A passive loop filter was considered for the specified loop noise bandwidths. Provision was made to achieve loop noisebandwidths

from 1.0 to 1000 cps with an active loop filter.

e. Tracking Loop Mechanization

The tracking loop mechanization is summarized briefly as follows:

(1) Phase Detector

Experimental effort was expended during Phase I to develop a high level broadband phase detector. The Linear S curve and bandwidth of this unit are indicated in figures 34 and 35. As shown, the unit is capable of developing an S curve of 40 volts peak to peak (with linear transfer of beat note output to signal level input) with a 5 MC video 3 DB bandwidth. As applied to the tracking loop, the 5 MC video bandwidth is not important, however, the linear S curve capability is essential to minimize noise biasing and retain a practical phase detector sensitivity at the tracking loop threshold.

(2) VCO

A precision 1 MC standard was fabricated in Phase I as a portion of the Linear S/N Summer. The long term stability was measured as 4 parts in  $10^{-8}$  over a 19 hour period. The short term stability was measured as 1.6 parts in  $10^{-11}$  referenced to an integration time of 1 sec. Two similar standards, arranged as VCOS, were phase compared by tuning to zero beat and the phase detector output filtered by a simulated  $[1 - H(\epsilon)]$  transfer with 2 BLO of 3.0 cps. The resultant phase noise was measured as 1.43 degrees peak. These results formed the basis for the tracking loop VCO specification.



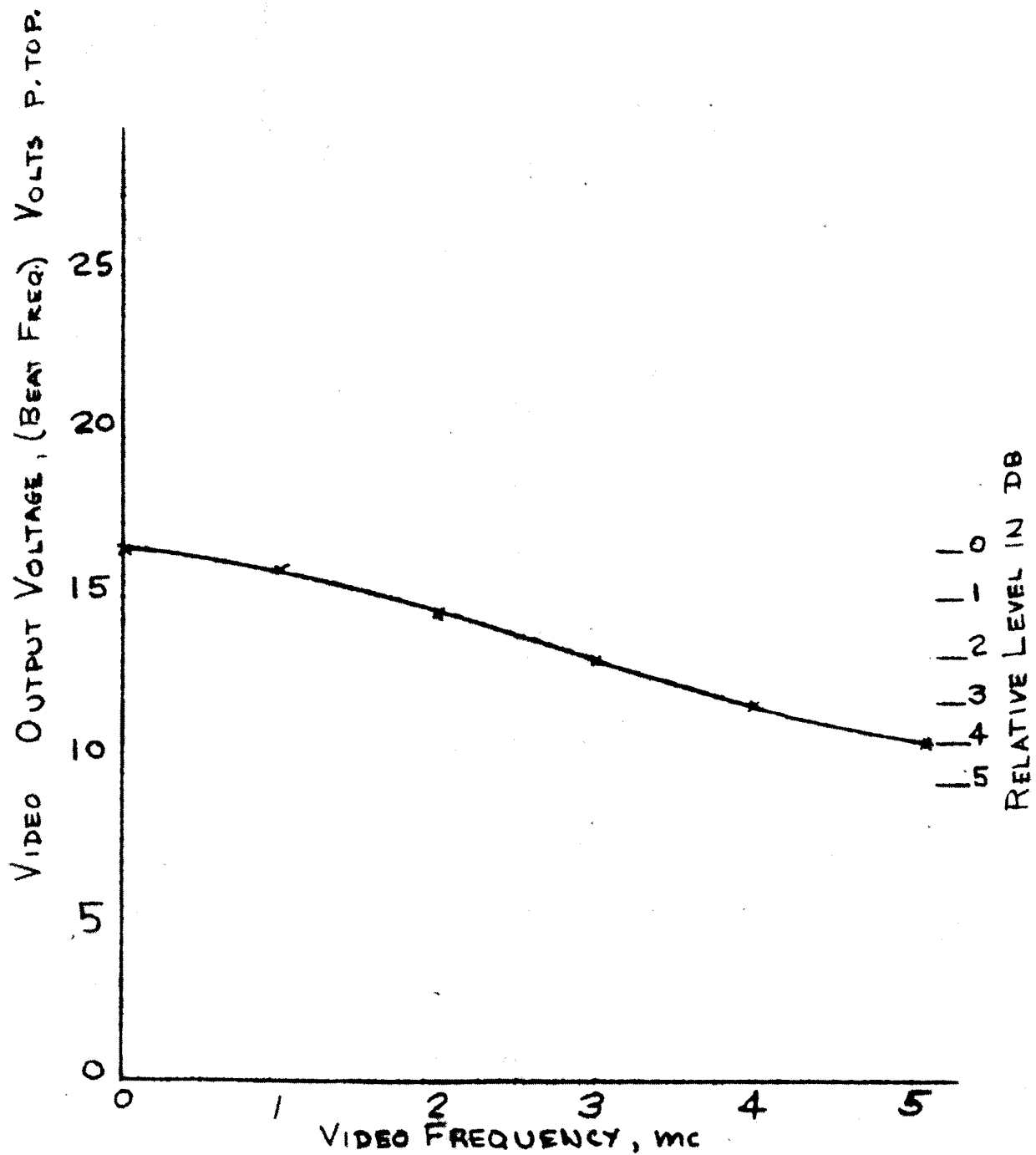
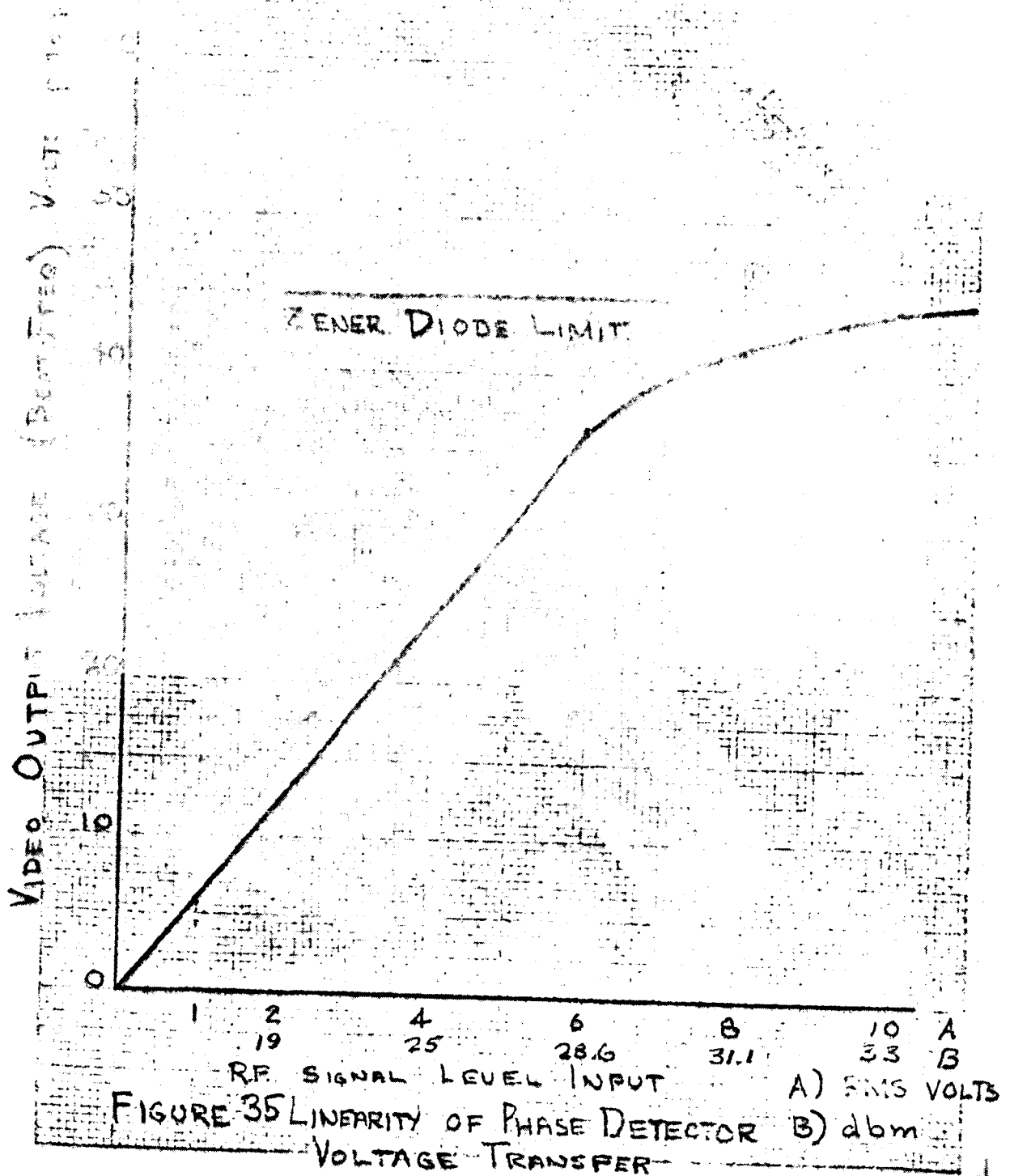


FIGURE 34 PHASE DETECTOR VIDEO BANDWIDTH CHARACTERISTICS



The center frequency of the tracking loop VCO will be 1 MC which in turn is multiplied to 60 MC to form the input balanced mixer reference.

The phase noise contribution of comparable  $\times 48$  frequency multipliers was measured as degrees peak in 2BLO of 3.0 cps.

(3) 10MC Reference Oscillator

The reference oscillator will be patterned after the characteristics of the tracking loop 1 MC VCO. However, the unit will be manually tuned and its 1 MC output multiplied to 10 MC.

(4) Narrow Band IF Amplifier

The basic Narrow Band IF Amplifier active element will be a feedback pair or doublet. This unit is a two stage feedback amplifier with approximately 40 DB of open loop power gain and 10 DB of closed loop gain. The closed loop 3 DB bandwidth extends from 1KC to 30 MC. Cascaded feedback pairs will provide the power gain assigned the narrow band IF amplifier 2KC crystal filter and the wideband amplifier 6 MC filter. Both units will be linear phase or Bessel filters. The group delay is the reciprocal of the 3 DB bandwidth. The group delay of the 6 MC demodulation channel filter is 160 u sec and the 2KC carrier tracking filter, 53 nanoseconds. The phase variation as a function of offset from center frequency is the product of group delay and frequency offset. Therefore, the carrier tracking IF output will track the wideband IF output only 30 cps offset from the 10 MCS center frequency. It is recognized that further phase divergence is attributed to the phase tracking characteristics of the demodulation channel and carrier tracking limiters. The demodulation channel limiters

of necessity have a larger noise limiting dynamic range than the tracking loop limiters. Therefore, the opportunity for phase shift between limiters as a function of limit levels exists. The latter source of phase tracking error can; however, be compensated by the phase shifters in each phase detector reference input. The phase shift characteristics of the basic limiter considered is outlined in Appendix F.

(5) Narrow Band IF Limiter

The gain, dynamic range, limit level and linear power capability of the tracking loop limiter is listed in the level diagram as 42DB, 36DB, ODBM and ODBM respectively. As outlined in Appendix F, a tunnel diode limiter and conventional limiter were fabricated and tested in Phase I. The tunnel diode limiter exhibited one half the phase shift (17 degrees) of the conventional limiter over a 60DB dynamic limit range. Further, the tunnel diode limiter yielded about one fourth the phase shift of the conventional emit as a function of temperature.

(6) Loop Amplifier

The carrier tracking amplifier was assigned the scale factor of 32  $\frac{\text{volts}}{\text{volt}}$ . The amplifier characteristics that were considered are listed as follows: a) bandwidth b) linearity c) dynamic range. d) stability e) noise figure f) overload recovery response. The Philbrick chopper stabilized SP-456 operational amplifier was selected.

(7) Balanced Modulator

The Input Mixer or Balanced Modulator is specified such that all spurious products that fall within the passband must be -60DB with respect to the desired output. Initially, a four term power series

representation of the mixer non-linearity was analyzed. The series was expanded assuming a mixer reference and a two tone signal input. The resultant terms were examined for spurious that fall within the pass-band as the two tone frequencies are varied across the input spectrum. The results indicated that if a perfect square law mixer can be fabricated no spurious terms appear in the passband. Further, if the optimum square law mixer is physically unrealizable (a valid assumption) the magnitude of the resulting in band spurious is a function of the order of the distortion and the level of the signal input. Summarizing the results, the mixer will exhibit a square law non-linearity (as close as possible) and the signal drive level will be minimized.

#### f. AGC Loop Design

The principal AGC loop specifications are indicated as follows:

"The AGC loop gain shall be greater than 20 over its entire operating range such that variation in the coherent receiver output, measured in the narrowband IF output shall not vary more than  $\pm 0.3\text{DB}$  for an input signal level variation of  $\pm 6\text{DB}$  about its design center. The AGC loop filter shall be a passive single pole RC low pass filter. The AGC loop shall have four (4) standard loop noise bandwidths of .01, 0.1, 1.0 and 10 cps."

The AGC loop filter time constants are expressed as a function of the open loop gain and noise bandwidths

$$\tau = \frac{G}{4 B_{LO}} \quad (40)$$

The open loop gain, G, is the dimension less product of

( $K_D$  = Receiver IF Gain  $\frac{DB}{Volt}$ ,  $K_a$  = coherent amplitude detector gain,  $\frac{volts}{DB}$  and  $G_1$  = loop amplifier gain  $\frac{volts}{volt}$  . ) The loop is non linear as the loop gain is a function of signal strength. A maximum open loop gain of 40 and minimum open loop gain of 20 was assumed. The scale factors assigned the loop components are summarized as follows:

$$K_a = 12 \frac{DB}{volt} \quad (41)$$

$$K_D = 0.03 \frac{volts}{DB} \quad (42)$$

$$G_1 = 110 \text{ volts/volt} \quad (43)$$

Table VIII lists a summary of the dynamic range of the various AGC loop voltages.

Table VIII AGC System Dynamic Voltage Ranges

1. Range of Input Signal Level (DEM)	-54 to -84
2. Regulated output variation over Input Signal Level Range (DEM) (0.3DB regulation for 6DB change of Input)	-8.24 to -9.74
3. AGC Quadrature Source (v peak)	-0.250 to -0.205
4. AGC Voltage Range Receiver Control Voltage	-7 to -2

g. AGC Loop Mechanization

The principal AGC loop components are listed as follows:

1. 50 MC Input Amplifier 2. Balanced Modulator 3. Narrow Band IF Amplifier 4. Quadrature Phase Detector 5. AGC Loop Amplifier.

The Balanced Modulator and Narrow Band IF amplifier were summarized in the section dealing with the carrier tracking loop. The Quadrature phase detector mechanization and dynamic range will be essentially the same as the carrier tracking loop phase detector. However, as applied to AGC loop the signal input to the Quadrature Phase Detector is prior to the limiter. Since the Quadrature Phase Detector is subjected to a S/N input of approximately -30DB the signal level must be low enough such that 3 $\sigma$  noise voltages are less than the phase detector reference. The maximum RMS noise voltage input to the quadrature phase detector is +20DEM. The unit will produce an output that is linear as a function of signal input up to signal input levels of +30DEM thus allowing 10DEM of linear range for noise excursion up to 3 $\sigma$ . The signal level input is approximately -10DEM and the DC output approximately 250 mv. The phase detector bandwidth must not degrade the 5KC AM modulation.

(1) Input Amplifier

The Input Amplifier produces the AGC scale factor of  $K_a (12 \frac{DB}{volt})$ . As mentioned briefly the active portion of the Input Amplifier will consist of four broadband feedback pairs each pair providing approximately 13DB of power gain. The attenuation will be assigned to either voltage sensitive diode attenuator interstage networks or current sensitive thermistor interstage attenuator. This arrangement exhibits less phase shift as a function of AGC control than controlling the transistor parameters directly.

## (2) AGC Loop Amplifier

The AGC loop amplifier was assigned a scale factor of  $110 \frac{\text{volts}}{\text{volt}}$ . The unit will be the same as the tracking loop amplifier (Philbrick SP-456). A minimum of two amplifiers will be required to provide stable operation with the scale factor of  $110 \frac{\text{volts}}{\text{volt}}$ . Further, an additional amplifier will be required (connected as a follower) to prevent loading of the single pole loop filter.

## h. Predetection Record and Playback

The predetection record output is derived from the wideband demodulation channel prior to the limiter. The original specification indicated that the predetection record spectrum, centered on 10 MC with 6 MC bandwidth was to be down converted and centered on 5 MC by multiplying the spectrum by a 15 MC carrier. Unfortunately this system allows spectrum overlap of any multiplier spectrum leak and the down converted spectrum. The system was modified to provide a stage of up conversion (spectrum centered on 10 MC multiplied by a 40 MC carrier yielding a spectrum centered on 50 MC) and a stage of down conversion (spectrum centered on 50 MC multiplied by a 45 MC carrier yielding a spectrum centered on 5 MC) to avoid spectrum overlap.

## 4. Phase Noise Instrumentation

The results of the Phase Noise Instrumentation investigation are outlined in Appendix G. The following is a summary of that effort. The Phase Noise Instrumentation system provides a measure of the standard deviation, mean and variance of the tracking loop VCO phase noise when subjected to various tests. The system is essentially a



phase comparator whereby the instantaneous VCO phase is compared to the phase of the 10 MC reference oscillator. The resultant noise spectrum is converted to baseband and also up converted for true RMS measurement. The sensitivity of the system is varied by changing the digital count, N, in figure 1, the system block diagram. The precision phase shifter provides a means of calibrating the output meters in degrees.

Ideally, the measurement system should be an order of magnitude more accurate than the system to be measured. The dividers were forecast as one of the principal sources of error within the measurement system. Therefore, the Statement of Work indicated the following: "Conduct experimentation to determine the most promising method of achieving short term stable frequency division."

The time jitter of high speed digital (toggle speed of 10 MC) counters was experimentally compared with the equivalent time jitter of a locked oscillator frequency multiplier system. The two systems are outlined in figures 36 and 37.

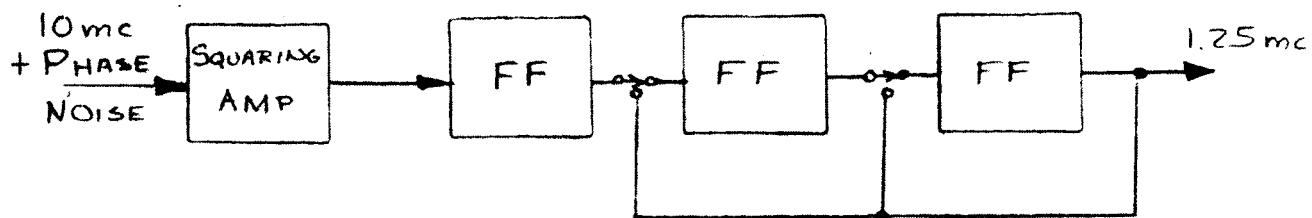


Figure 36. Frequency Division with Bistable Multivibrators

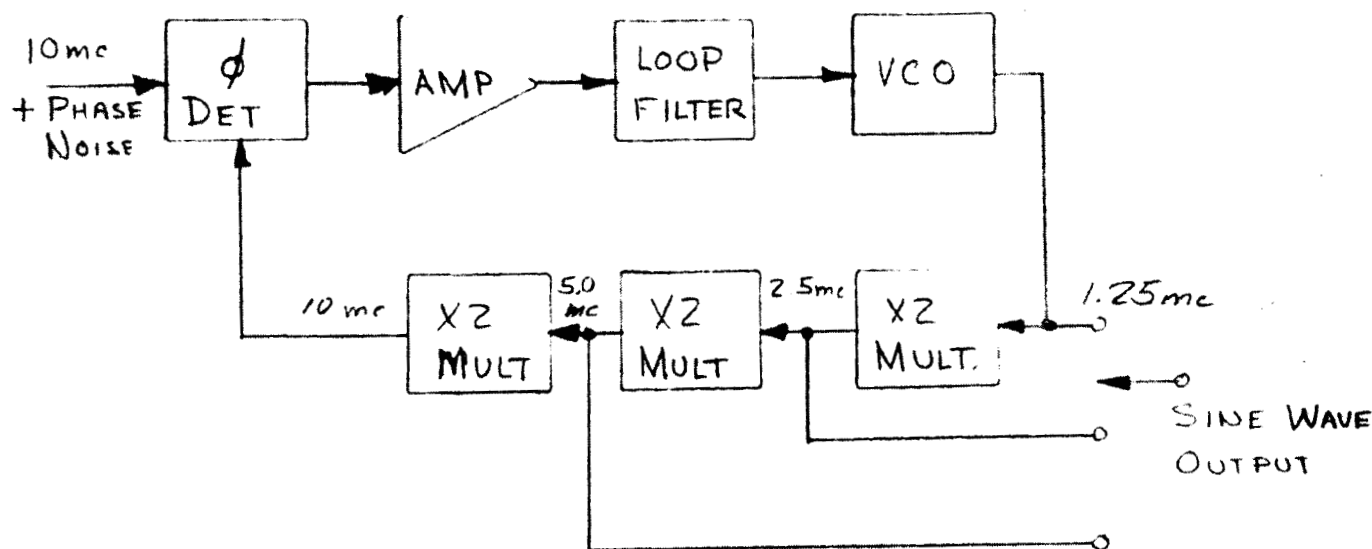


Figure 37. Frequency Division with Phase Locked Oscillator

The time jitter, or uncertainty of zero crossings, of the binary divider is basically determined by the toggle speed of the flip flop. The relative time jitter of two 3 bit grey code counters was measured with a system whose resolution was 0.2 nanoseconds (0.71 degrees at 10 MC). The resultant time jitter was too small to measure. Conversely, the relative phase noise of comparable frequency multipliers was measured as outlined in figure 38.

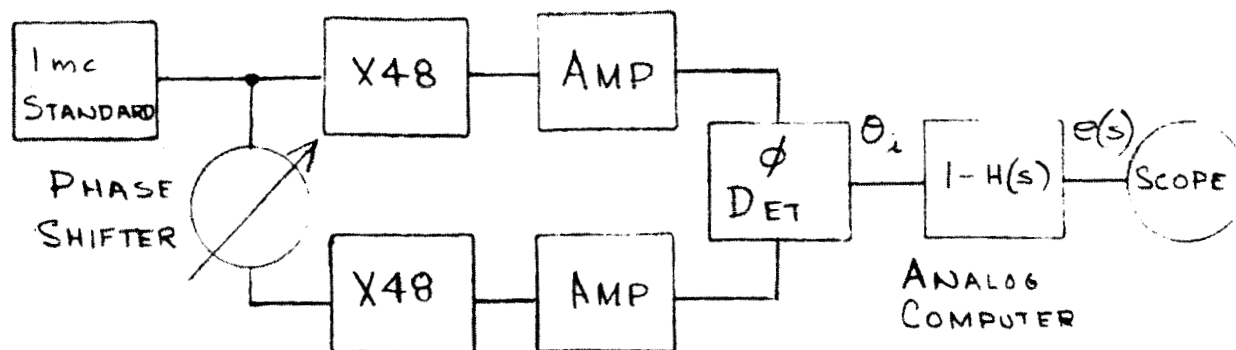


Figure 38 Multiplier Phase Noise Measurement

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The carrier tracking loop corrects the VCO phase noise in accordance with the transfer of  $1 - H(s)$ . Therefore, as shown in figure 38 the low frequency components of the phase noise were filtered by  $(1 - H(s))$ ,  $2BLO = 3.0$  cps). The phase detector was calibrated and the resultant phase noise was measured as 1.43 degree peak at 48 MC. Assuming a linear translation of phase jitter with frequency multiplication, the phase jitter of the 5 MC output of figure 37 attributed to the multipliers becomes 0.148 degrees or .08 nanoseconds. On this basis there is little to choose between the two systems. However, additional sources of phase noise within the loop were not measured (admittedly the phase detector and loop amplifier noise contributions experience the least amount of attenuation). However, the binary counter system was selected for the following reasons: 1) Simplicity 2) No acquisition problem 3) Thin Film 50 MC Flip Flops are now available.

66-435

D. FM/AM Sub System

The FM/AM Sub System is outlined in figure 1, the R.F. Test Console Functional Block Diagram. The Sub System consists of the FM Transmitter, AM Transmitter, Conventional and Phase Lock FM Receiver.

1. FM/PM Transmitter

Portions of the FM Modulator and PM Modulator utilize the same components. The specification does not require simultaneous FM and PM Transmission; therefore, some units of both transmitters will be the same.

a. F.M. Transmitter

The details of the F.M. Transmitter are outlined in Appendix H. The following constitutes a summary of Appendix H.

(1) Summary of Specifications

The Frequency Modulator requirements are summarized as follows:

Summary of Specifications

- |                                    |  |
|------------------------------------|--|
| (a) Transmitter Center Frequency   | 50mc manually tunable $\pm$ 500 cps  |
| (b) Frequency Response             | $\pm$ 0.1 DB from 50 cps to 100 kc<br>and $\pm$ 0.5 DB from 3 cps to 50 cps<br>and 100 kc to 500 kc  |
| (c) Frequency Deviation            | $\pm$ 500 kc, maximum modulation<br>index 512 in AFC Mode  |
| (d) Mode                           | AFC (Frequency Response 3 cps<br>to 500 kc)<br>Non-AFC (Frequency Response<br>DC to 500 kc)  |
| (e) Residual F.M.                  | TX/RX pair, 15 cps in AFC Mode<br>60 cps in Non-AFC Mode   |
| (f) Static Linearity<br>TX/RX Pair | $\pm$ 0.5% over full-scale deviation<br>with non AFC TX and either RX<br>(above and beyond inherent<br>sinusoidal phase detector<br>non-linearity) |

- (g) Dynamic Linearity TX/RX pair + 1.0 percent in AFC and non-AFC Mode (above and beyond inherent sinusoidal phase detector non-linearity)
- (h) Deviation Linearity TX/RX pair sufficiently linear to meet the static and dynamic linearity requirements

(2) Summary of Design Objectives

(a) AFC Loop Characteristics

- (1) Closed Loop Response - Butterworth
- (2) Equivalent Closed Loop Butterworth cut off frequency - 2.5 mcs
- (3) Variation in closed loop group delay over 500 kc baseband - 3 nanoseconds

(b) AFC Loop Characteristics

- (1) Loop Natural Frequency - 57.3 rad/sec
- (2) Loop Gain - - - 107.8 DB
- (3) Loop Rejection of Phase Detector Feedthrough, -60 DB
- (4) Pre-emphasis Transfer Function

$$K \left[ \frac{\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n} s + 1}{s^2} \right]$$

(3) AFC Loop

A Simplified Block Diagram of the AFC Loop is shown in

figure 39.

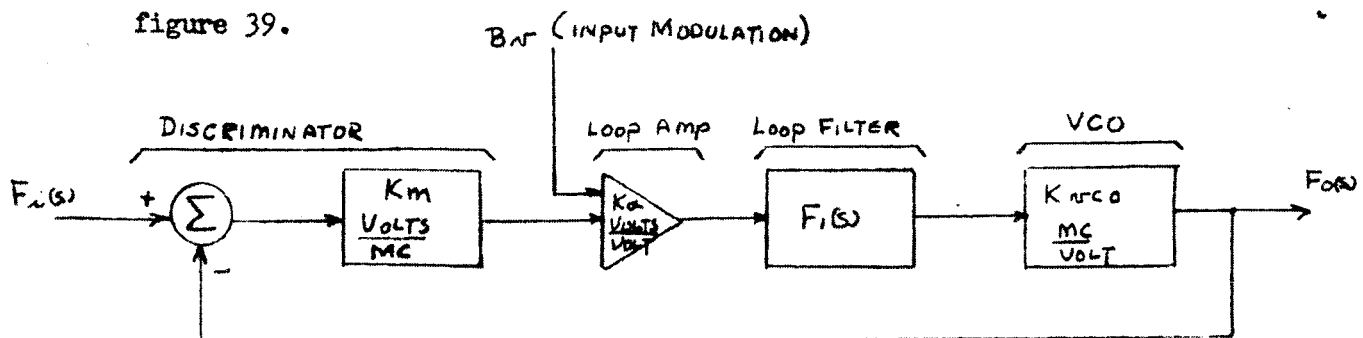


Figure 39. Simplified Model, AFC Loop

The transfer function  $\frac{F_o(s)}{B_m}$  is indicated by equation 44

$$\frac{F_o(s)}{B_m} = \frac{K_a K_{vco} F_1(s)}{1 + K_m K_a K_{vco} F_1(s)} \quad (44)$$

$$\text{Let } K_p = K_m K_a K_{vco} ; K_m = 1$$

$$\frac{F_o}{B_v}(s) = \left[ \frac{1}{1 + \frac{1}{K_p F_i(s)}} \right] \quad (45)$$

$$\text{Let } F_i(s) = \frac{1}{\left(\frac{s}{\omega_1} + 1\right) \left(\frac{s^2}{\omega_{n0}^2} + 1\right)^2} \quad (46)$$

$$\frac{F_o}{B_v}(s) = \frac{1}{\frac{1}{K_p} \left(\frac{s}{\omega_1} + 1\right) \left(\frac{s^2}{\omega_{n0}^2} + \frac{2}{\omega_{n0}} s + 1\right) + 1} \quad (47)$$

$$\frac{F_o}{B_v}(s) = \frac{1}{\frac{1}{K_p \omega_1 \omega_{n0}^2} s^3 + \frac{1}{K_p} \left(\frac{2}{\omega_1 \omega_{n0}} + \frac{1}{\omega_{n0}^2}\right) s^2 + \frac{1}{K_p} \left(\frac{1}{\omega_1} + \frac{2}{\omega_{n0}}\right) s + \frac{1}{K_p} + 1} \quad (48)$$

The transfer function of a 3 Pole Butterworth filter is of the form:

$$F(s)' = \frac{1}{\left(\frac{s}{\omega_n} + 1\right) \left(\frac{s^2}{\omega_n^2} + \frac{2\epsilon}{\omega_n} + 1\right)} = \frac{1}{\left(\frac{1}{K_p} + 1\right) \frac{s^3}{\omega_n^3} + \left(\frac{1}{K_p} + 1\right) \left(\frac{2\epsilon + 1}{\omega_n}\right) s^2 + \left(\frac{1}{K_p} + 1\right) \left(\frac{2\epsilon + 1}{\omega_n}\right) s + \frac{1}{K_p} + 1} \quad (49)$$

Equating coefficients of like powers of s of equations 48 and 49 the following results

$$(K_p + 1) \omega_1 \omega_{n0}^2 = \omega_n^3 \quad (50)$$

$$\left(\frac{2}{\omega_1 \omega_{n0}} + \frac{1}{\omega_{n0}^2}\right) = (K_p + 1) \left(\frac{2\epsilon + 1}{\omega_n^2}\right) \quad (51)$$

$$\left( \frac{1}{\omega_1} + \frac{2}{\omega_{n0}} \right) = (K_p + 1) \left( \frac{2\xi + 1}{\omega_n} \right) \quad (52)$$

The open loop gain,  $K_p$ , was assigned a realistic value ( $K_p = 50$ ) as dictated by the hardware limitations. The loop filter's poles  $\omega_1$  and  $\omega_{n0}$  were solved as a function of the closed loop Butterworth cut off frequency,  $\omega_n$ , (and open gain  $K_p$ ) as indicated by equations 53 and 54.

$$\omega_{n0} = 0.99 \omega_n \quad (53)$$

$$\omega_1 = 2(\omega_n - \omega_{n0}) \quad (54)$$

The normalized amplitude response, phase response and group delay of equation 49 (3 pole Butterworth) was tabulated on the digital computer. The Butterworth cut off frequency ( $\omega_n$ ) was selected to yield a relatively constant group delay over the modulation base band, 500 kc. The cut off frequency was selected as,  $\omega_n = 5\pi \cdot 10^6$  rad/sec. The change in group delay over the 500 kc baseband is 3 nanoseconds and the droop in amplitude response, 0.0003 DB. Figure 40 indicates the resultant open loop and closed loop amplitude response, figure 41 indicates the resultant group delay. Figure 42 shows the Root Locus Plot.

Figure 43 indicates a simplified model of the AFC loop with inter-modulation(non linearities) sources simulated as separate inputs. The loop's influence on VCO non linearity is shown by equation 55.

$$\frac{f_o(s)}{I_{arco}} = \frac{1}{K_m K_f} \left[ \frac{K_p}{K_p + F\omega} \right] = \frac{1}{K_m K_f} \left[ \frac{\left( \frac{s}{\omega_1} + 1 \right) \left( \frac{s}{\omega_{n0}} + 1 \right)^2}{\left( \frac{s}{\omega_n} + 1 \right) \left( \frac{s^2}{\omega_n^2} + \frac{2\xi s}{\omega_n} + 1 \right)} \right] \quad (55)$$

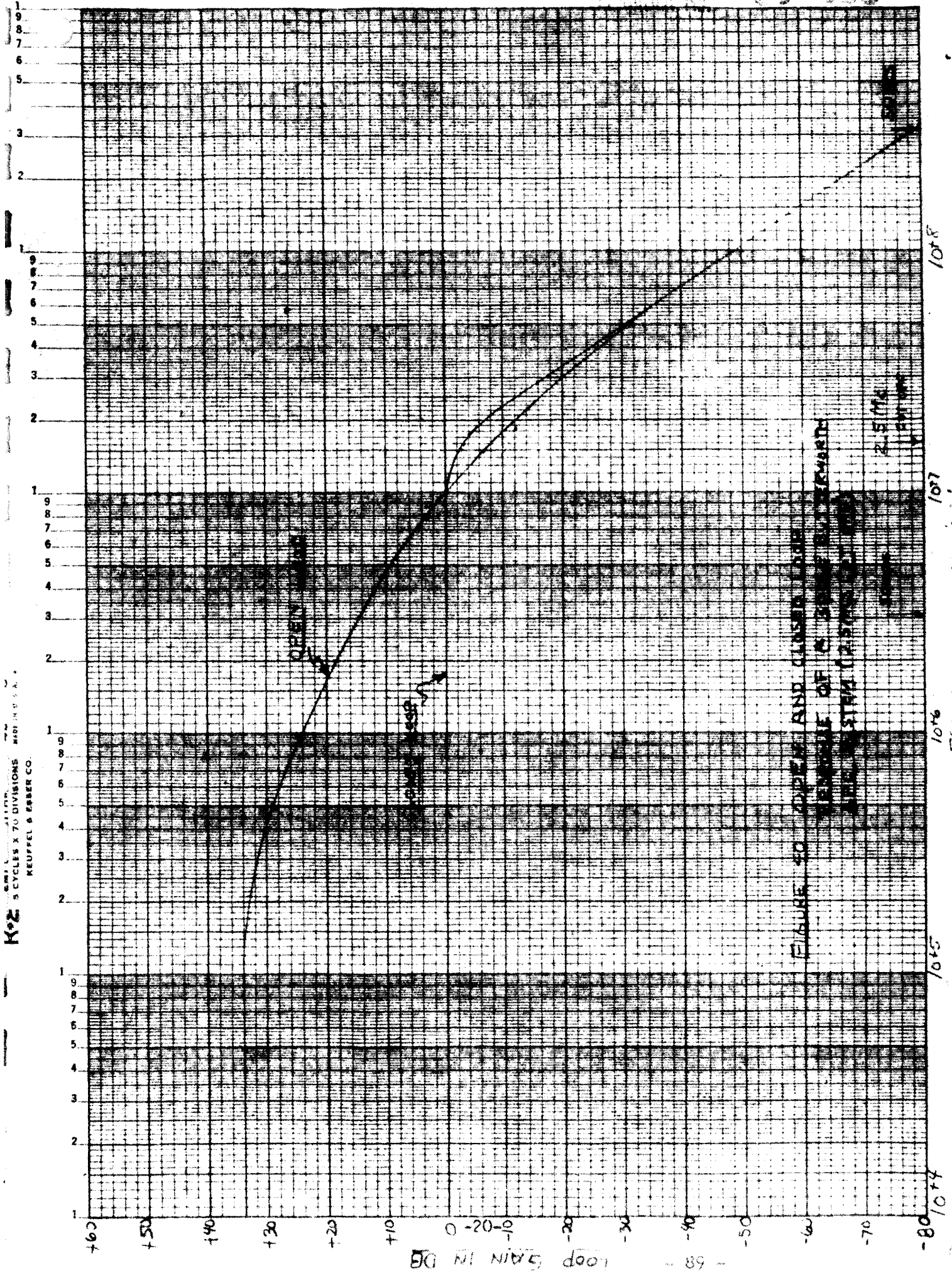
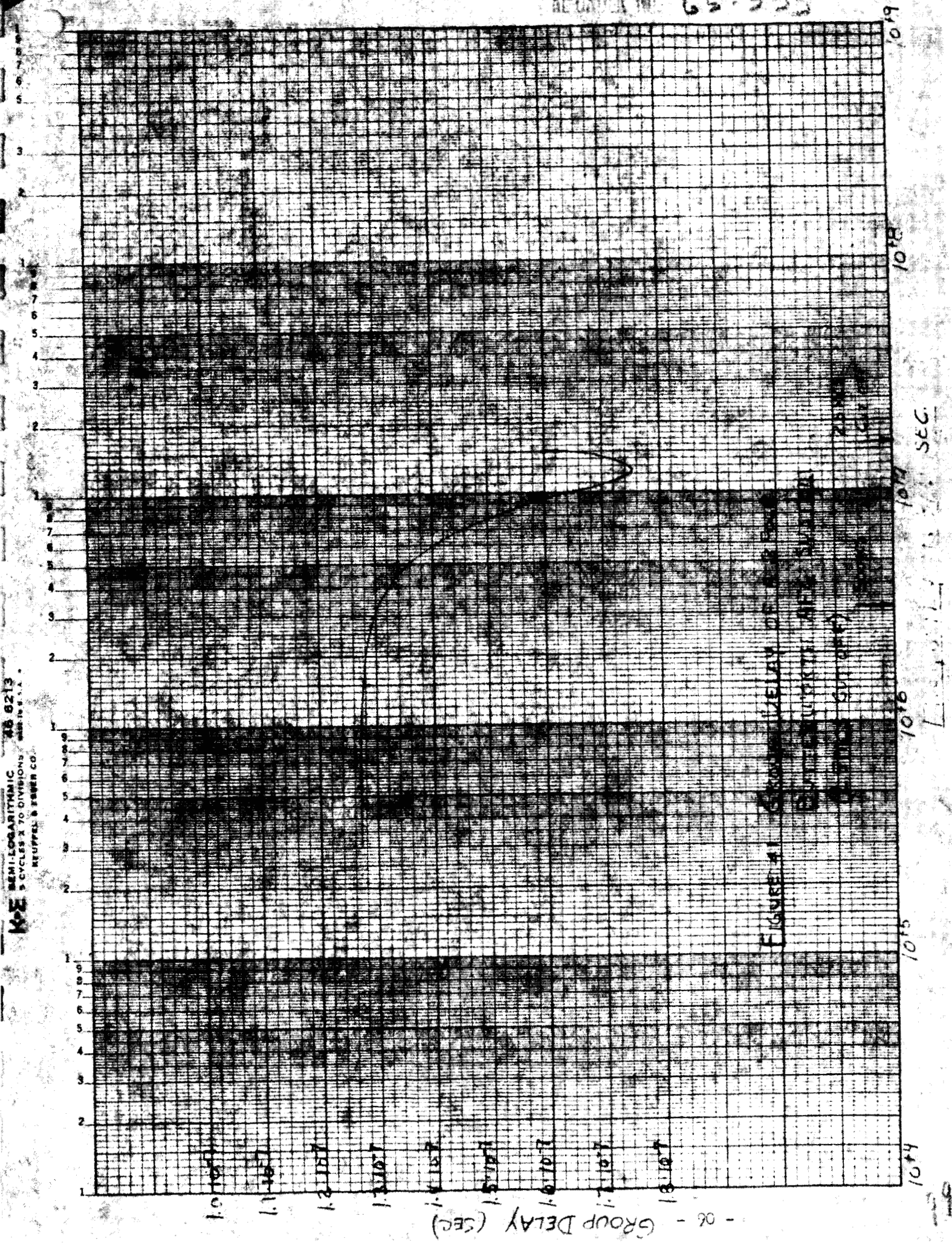


FIGURE 40. OPEN AND CLOSED LOOP  
GAIN OF A BJT BJT BJT  
BJT BJT BJT BJT

FREQUENCY





NOTE: OPEN LOOP DOUBLE POLE AT  $0.99 \omega_n$  BECOME COMPLEX BUTTERWORTH POLES IN CLOSED LOOP RESPONSE

OPEN LOOP POLE AT  $2.02 \omega_n$  BECOMES REAL POLE AT  $\omega_n$

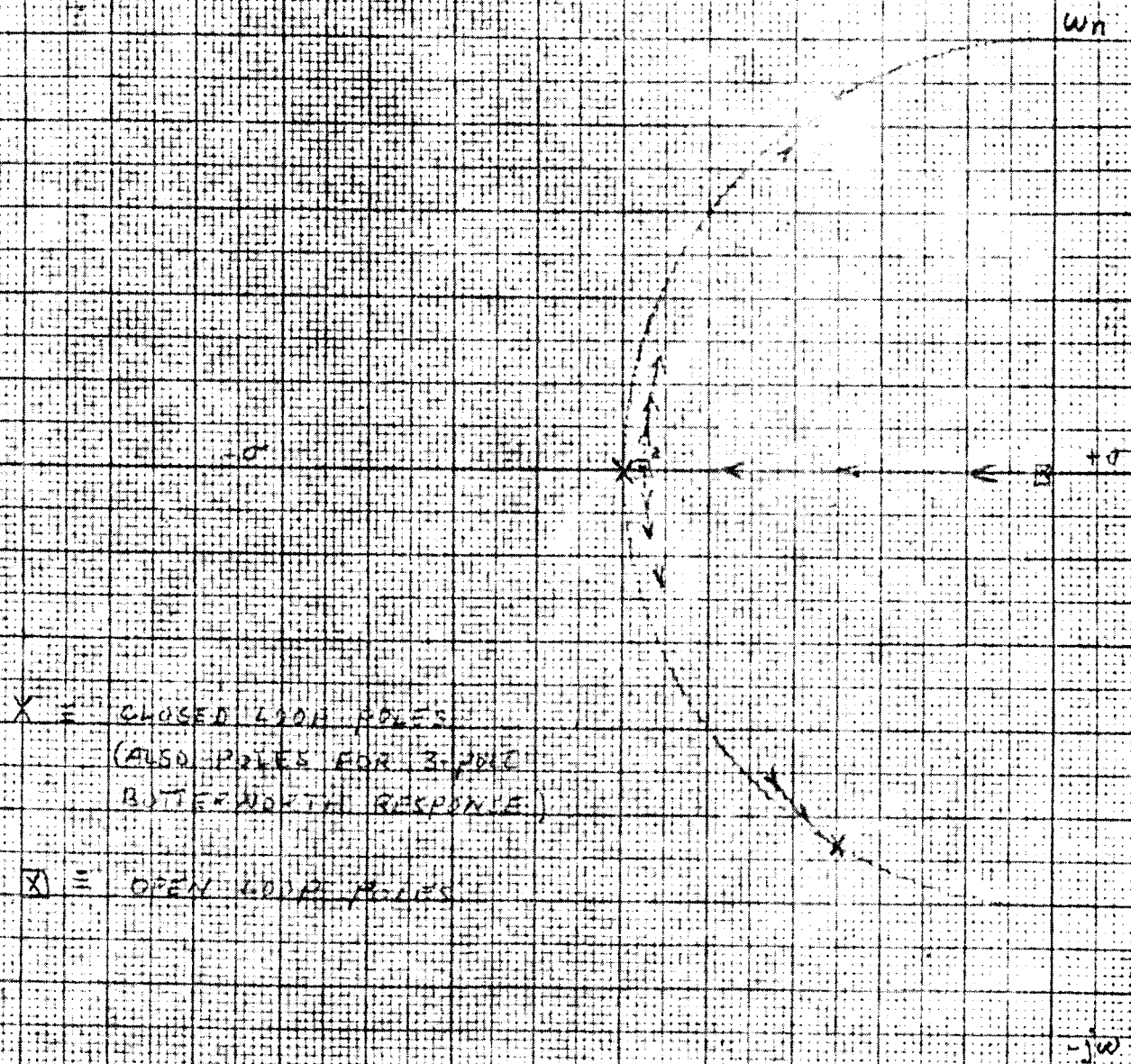
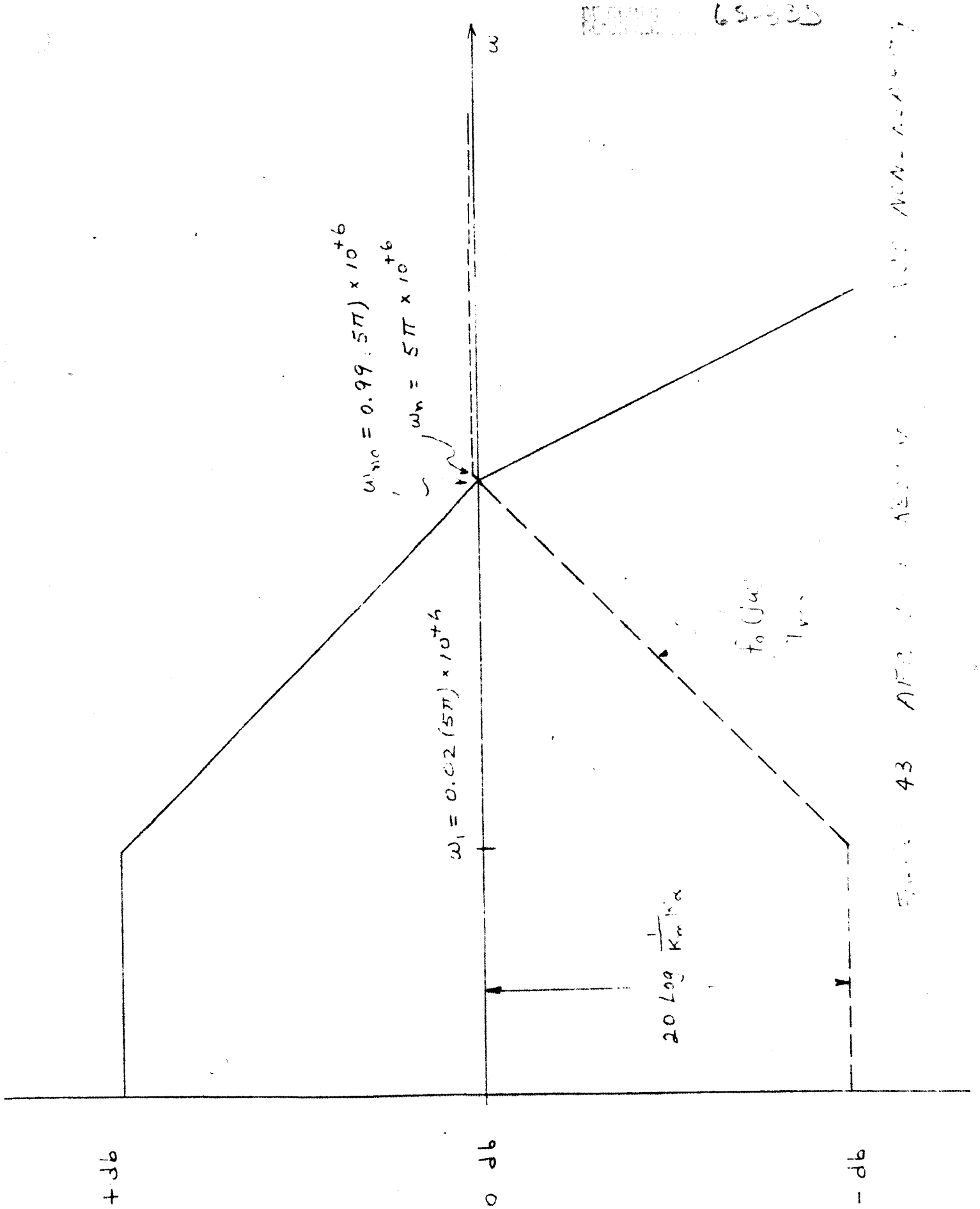


FIGURE 42 ROOT LOCUS OF THREE-POLE BUTTERWORTH AEC SYSTEM



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43 AFB 100 NON-RE...

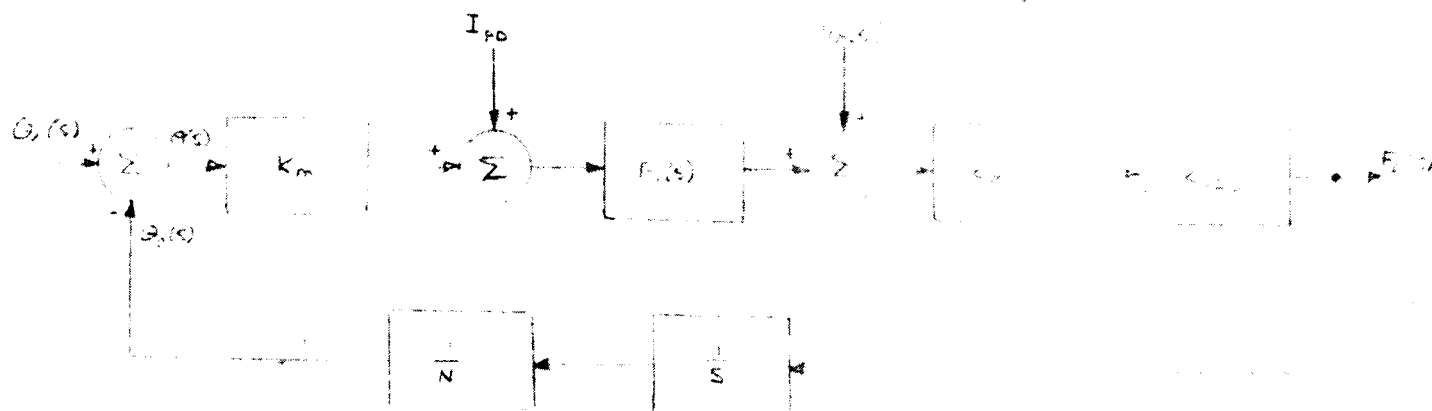


Figure 44. Simplified Diagram, Locked Oscillator Frequency Modulator

As shown by equation 50 and figure 43 the loop attenuates as the VCO non linearity (i.e. the discriminator linearity is transferred to the VCO within the constraints of loop gain). The loop performs no correction of the discriminator non linearity. Therefore, the AFC loop requires a linear discriminator as outlined in Appendix 1 pages 30 thru 36. The AFC loop improves the VCO linearity; however, the unmodulated VCO center frequency is a function of the AFC loop gain and reference frequency stability. The AFC reference of course is provided by the discriminator. The discriminator referenced earlier yields 0.3% linearity over a 20% bandwidth. However, the reference stability is unacceptable. The reference instability (rate of change of VCO center frequency) is detected as residual FM in the receiver. Therefore, the narrowband auxiliary APC loop was added to the system to stabilize the VCO center frequency.

#### (4) APC Loop

A simplified block diagram of the APC loop is shown in figure 44.

The AFC loop has been replaced by an equivalent linear VCO. To be exact, the AFC loop should be replaced with a unit whose transfer function is the AFC closed loop transfer function. Alternately, the AFC loop can be retained and the transfer function of the APC loop written as a function of both loops using Mason's rules for dealing with multi loop systems. However, the AFC closed loop transfer function is not frequency sensitive, at least over the frequency range of interest of the APC loop, and the approximation is valid. Referring to figure 44 the transfer function of output frequency,  $F_o(s)$ , to input modulation,  $V_m$ , is expressed by equation 56.

$$\frac{F_o(s)}{V_m} = \frac{K_{\alpha} K_{VCO}}{1 + \frac{K_m K_{\alpha} K_{VCO} F(s)}{N s}} \quad (56)$$

$$\text{Let } K_v = \frac{K_m K_{\alpha} K_{VCO}}{N} \quad \text{and } F(s) = \frac{z_2 s + 1}{z_1 s} \quad (57)$$

$$\frac{F_o(s)}{V_m} = \frac{N}{K_m} \left[ \frac{z_1 s^2}{z_2 s^2 + z_1 s + 1} \right] \quad (58)$$

$$\text{Let } z_1 = \frac{K_v}{\omega_n^2} \quad z_2 = \frac{2\zeta}{\omega_n} \quad (59)$$

$$\frac{F_o(s)}{V_m} = N K_{\alpha} K_{VCO} \frac{\frac{s^2}{\omega_n^2}}{\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n} s + 1} \quad (60)$$

Let  $\xi = 0.707$  and  $s = j\omega$

The response of equation 62 is

$$\left| \frac{F_o}{V_m} \right|_{s=j\omega} = N K_\alpha K_{vco} [G(s) \cdot G(-s)]^{1/2} \quad (61)$$

$$= N K_\alpha K_{vco} \left[ \frac{\frac{\omega^2}{\omega_n^2}}{\sqrt{\left(\frac{\omega}{\omega_n}\right)^4 + 1}} \right] \quad (62)$$

Figure 46 indicates a plot of equation 64. The highpass characteristic of equation 64 is not compatible with the amplitude response specification ( $\pm 0.1$  DB from 50 cps to 100 KCS and  $\pm 0.5$  DB from 3 cps to 50 cps and 100 KC to 500 KC) if the lower bound of the baseband approaches  $\omega_n$ . Appendix H includes an active pre-emphasis network whose transfer function is the inverse of equation 60 extending the lower corner response of figure 45.

Aside from the transfer of  $\frac{F_o}{V_m}(s)$  and the form of the pre-emphasis network, the APC loop's influence on the phase detector harmonics and reference frequency feedthrough are of interest. Refer to figure 44. The phase detector harmonics are simulated by an additional input,  $I_{PD}$ . A linear system is assumed and superposition applied. The transfer,  $\frac{F_o}{V_m}(s)$ , is listed in equation 56. The transfer  $\frac{F_o}{I_{PD}}(s)$  is indicated by equation 63.

$$\frac{F_o}{I_{PD}}(s) = \frac{K_\alpha K_{vco} F_i(s)}{1 + \frac{K_m K_\alpha K_{vco} F_i(s)}{Ns}} \quad (63)$$



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TYPE 5 CYCLES X 10 DIVISIONS MADE IN U.S.A.  
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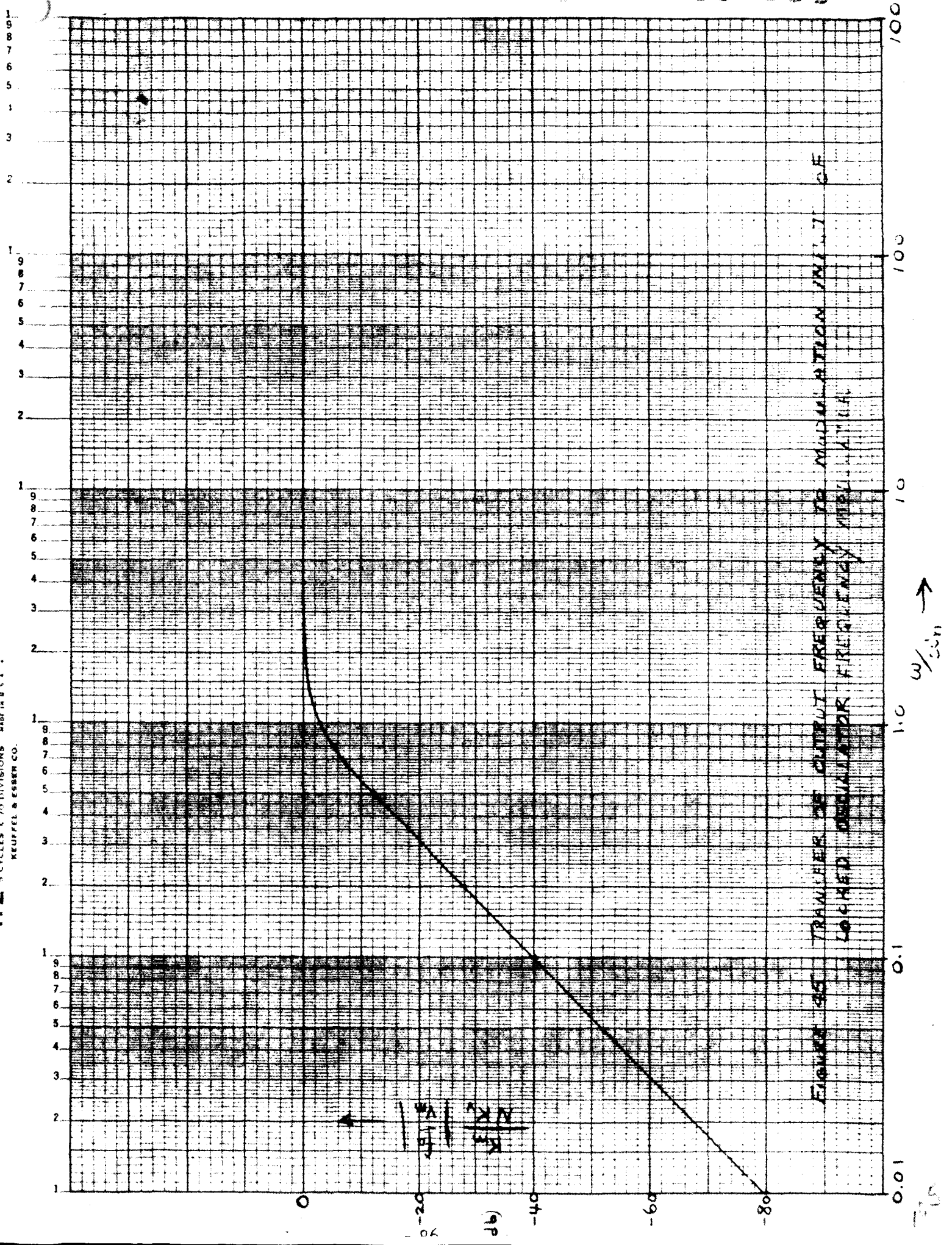


FIGURE 35 TRANSFER OF OUTPUT FREQUENCY TO MODULATION FREQUENCY OF LOCKED OSCILLATOR FREQUENCY

Equation 63 divided by equation 56 yields

$$\frac{V_m}{I_{PD}}(s) = F(s) \quad (64)$$

Equation 64 indicates that the relative magnitude of  $V_m$  to  $I_{PD}$  is determined by the APC loop filter. The loop filter is of the form,

$\frac{Z_2 s + 1}{Z_1 s + 1}$ , a simple lag lead configuration. If the lower frequency component of (the phase detector feedthrough) is greater than  $\frac{1}{Z_2}$  and if  $Z_1$  equals  $1000 Z_2$ ,  $I_{PD}(j\omega)$  is -60dB with respect to  $V_m$ .

The loop parameters ( $G$ ,  $Z_1$ ,  $Z_2$ ,  $\omega$ , etc) are determined in Appendix H. The loop gain and resonant frequency were established to constrain the phase error to 1/10 radian when either the reference frequency detuning rate or VCO drift rate subject the APC loop to a frequency ramp of  $50 \frac{\text{cycles}}{\text{sec}^2}$ . The parameters of interest are listed as follows:

$$G = \frac{2\pi K_m K_a K_{VCO}}{N} = \frac{(6.28)(1)(10)(2 \times 10^6)}{512} = 2.45 \times 10^6 \quad (65)$$

$$Z_1 = R_1 C = \frac{G}{\omega_n^2} = 39.4 \text{ sec} \quad (66)$$

$$Z_2 = R_2 C = \frac{\sqrt{2}}{\omega_n} = 0.0179 \text{ sec} \quad (67)$$



Appendix H includes a section dealing with hardware mechanization and system power levels.

(5) AM Transmitter

The amplitude Modulator must be capable of amplitude modulating the angle modulated carrier (either FM or FM)  $\pm$  50 percent in voltage. The frequency response of the amplitude modulator must be constant within 0.1DB from DC to 5.0KC, the linearity within  $\pm$  1.0 percent and the incidental angle modulation negligible. Appendix H includes preliminary test results of the General Radio Balanced Modulator Model 1000-P6 which is applicable.

2. F.M. Receiver

Appendix I of this report contains the details of the FM Receiver study. The following constitutes a summary of that effort.

a. FM Receiver Block Diagram

The portion of the statement of work pertaining to the FM receiver is summarized as follows: "Perform an analysis of a FM receiver which satisfies the requirements of JPL specification GPG-15062-DSN par. 3.5.2. The analysis shall include the discriminator linearity requirements and the loop parameters of the phase locked F.M. discriminator. The analysis shall yield a detailed block diagram indicating impedance levels, filter bandwidths and the dynamic range of signal and noise voltages".

Figure 1 includes the F.M. Receiver block diagram. The configuration is the same as outlined in the JPL specification. Figure 1.6 indicates a detailed block diagram of the FM Receiver indicating signal and noise power levels, limit levels and amplifier gains.



a. Limiter Chain Signal and Noise Power Levels

Figure 46 indicates the input signal to noise power levels referenced to the maximum and minimum input filter bandwidths. The Input Filter's 3DB bandwidths are specified as 10 percent of the noise bandwidths. The three pole Butterworth filter meets the noise bandwidth requirement; however, this filter exhibits a 45 nanosecond change in group delay from approximately one tenth to one half the 3DB bandwidth. Conversely, the change in group delay of a Bessel Filter over the same percentage bandwidth is negligible; however, the noise bandwidth and 3DB bandwidth of the latter unit is not compatible with the spec. It has been suggested that an allpass phase equalizing network be used in conjunction with the Butterworth filter to achieve constant group delay and specified noise bandwidth. A realizable phase corrective network that yields an overall phase response comparable to a Bessel response is not realizable. Therefore, a Bessel Filter is recommended.

As shown in figure 46, 60DB of limiting follows the input filter. A basic limiting stage with approximately 7.5DB of limiting and gain is described in Appendix I. As shown in figure 46 each limiter stage amplifier must have a linear RMS power capability of 0DBM. A buffer amplifier with one sigma linear capability of +20DBM follows the limiter chain and provides the required phase detector drive level.

b. Phase Lock F.M. Discriminator

The phase lock discriminator characteristics are determined by the specified loop information bandwidth and open loop gain. Three standard loop information bandwidths are specified; namely, 1, 30, and 300KC. The open loop gain must be sufficient to constrain the static loop phase error to less than 10 degrees peak under conditions of maximum transmitter deviation.

The open loop gain is indicated by equation 68

$$G = \frac{2\pi\Delta f}{\sin 10^\circ} \quad (68)$$

The maximum transmitter deviation is 500 KCS; therefore, the minimum open loop gain is  $1.81 \times 10^7$  or 145DB. The minimum above threshold gain was computed in Appendix I based on sufficient threshold gain ( $\alpha_0$ ) to constraint the static phase error to 10 degrees at maximum transmitter deviation. The threshold limiter suppression  $\alpha_0$  is 0.055 [S/N = -24.2DB in predetection bandwidth]; therefore, applying this logic the minimum open loop gain is 170DB above threshold and 145DB at threshold. One may argue that the 10 degree static phase error is meaningless at threshold as the VCO is out of lock about one third of the time. However, the loop filter time constants were computed in Appendix I based on the larger loop gain. The basic relationships are outlined in equations 33 thru 39 of this report.

### c. Conventional Discriminator

The system specifications that influence the discriminator characteristics are listed as follows:

1. Static and dynamic linearity
2. Distortion (Discriminator Balance)

The delay line discriminator shown in figure 47 exhibits a linear transfer of output voltage to input frequency. The discriminator characteristic for sinewave inputs (reference figure 47) are listed as follows:

$$\phi_d = \pi \frac{f}{f_0} \quad (69)$$

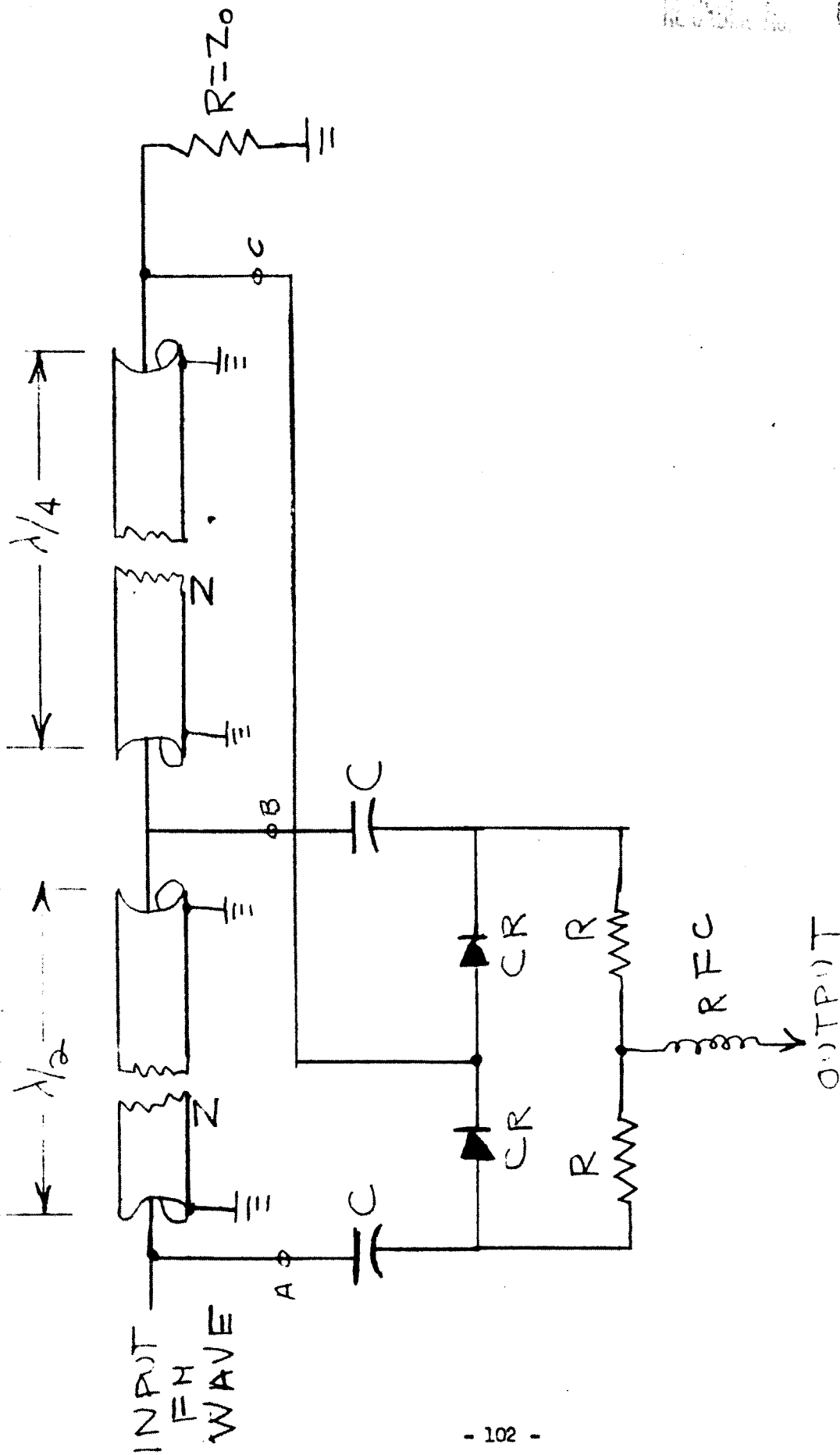


FIG. 47 DELAY LINE FREQUENCY DISCRIMINATOR

$$\phi_c = \frac{3}{2} \pi \frac{f}{f_0} \quad (70)$$

The voltages at point A, B, and C may be written as follows:

$$V_A = \cos \omega t \quad (71)$$

$$V_B = \cos (\omega t - \phi_B) \quad (72)$$

$$V_C = \cos (\omega t - \phi_C) \quad (73)$$

The first detector yields an output voltage proportional to the difference between  $V_A$  and  $V_C$

$$V_{A-C} = \cos(\omega t - \phi_B) - \cos(\omega t - \phi_C) = -2 \sin(\omega t - \frac{\phi_C}{2}) \sin \frac{\phi_C}{2} \quad (74)$$

The second peak detector output is:

$$V_{B-C} = \cos(\omega t - \phi_A) - \cos(\omega t - \phi_C) = -2 \sin(\omega t - \frac{\phi_A + \phi_C}{2}) \sin(\frac{\phi_C}{2} - \frac{\phi_A}{2}) \quad (75)$$

One detector output is nearly equal to the peak of  $V_{A-C}$  ( $V_1$ ) and the other the peak of  $V_{B-C}$  ( $V_2$ )

$$V_1 = \sin \frac{\phi_C}{2} \quad (76)$$

$$V_2 = \sin(\frac{\phi_C}{2} - \frac{\phi_A}{2}) \quad (77)$$

The outputs are summed (with opposite polarity) and become

$$V_1 - V_2 = K \sin \frac{\phi_n}{4} \cos \frac{\phi_c}{2} \quad (78)$$

Relating phase and frequency  $B = 180 f/f_0$

$$V_1 - V_2 = \sin 45 f/f_0 \cos 90 f/f_0 \quad (79)$$

Equation 79 was computer (to four place accuracy) for values of  $\frac{f}{f_0} = \frac{52}{45}$

to  $\frac{f}{f_0} = \frac{64}{45}$ . The linearity is within .05%. The unit has been built and tested. The results verify equation 79.

#### 6. Frequency Synthesizer Subsystem

The frequency Synthesizer Subsystem is indicated in figure 48. There is no separate appendix dealing with the Frequency Synthesizer; however, the principal portions of the unit have been described in the P.M. Receiver Subsystem. The short term and long term frequency stability of the various frequency multipliers (50 mc source) were related to the specified carrier tracking loop noise error.

The 64 mc synthesizer output is provided to down convert the S/N Summer output to 15 mc for spectrum display. The 55 mc output is used to down convert the 50 mc FM receiver spectrum for predetection record at 5 mc. Additional frequencies, 50.01, 50.02, 50.05, 50.1, 50.2 and 50.5 mcs, are provided to down convert the S/N summer output to video for display on the Spectrum Analyzer. The latter frequencies are generated as shown in figure 49 by phase lock techniques. The active filter system shown is required to suppress all spurious 60DB for the 50.01, 50.02 and 50.05 mc frequencies. The 50.1, 50.2, 50.5 and 55.0 mcs frequencies can be filtered properly either with the phase lock system shown or with crystal filters.

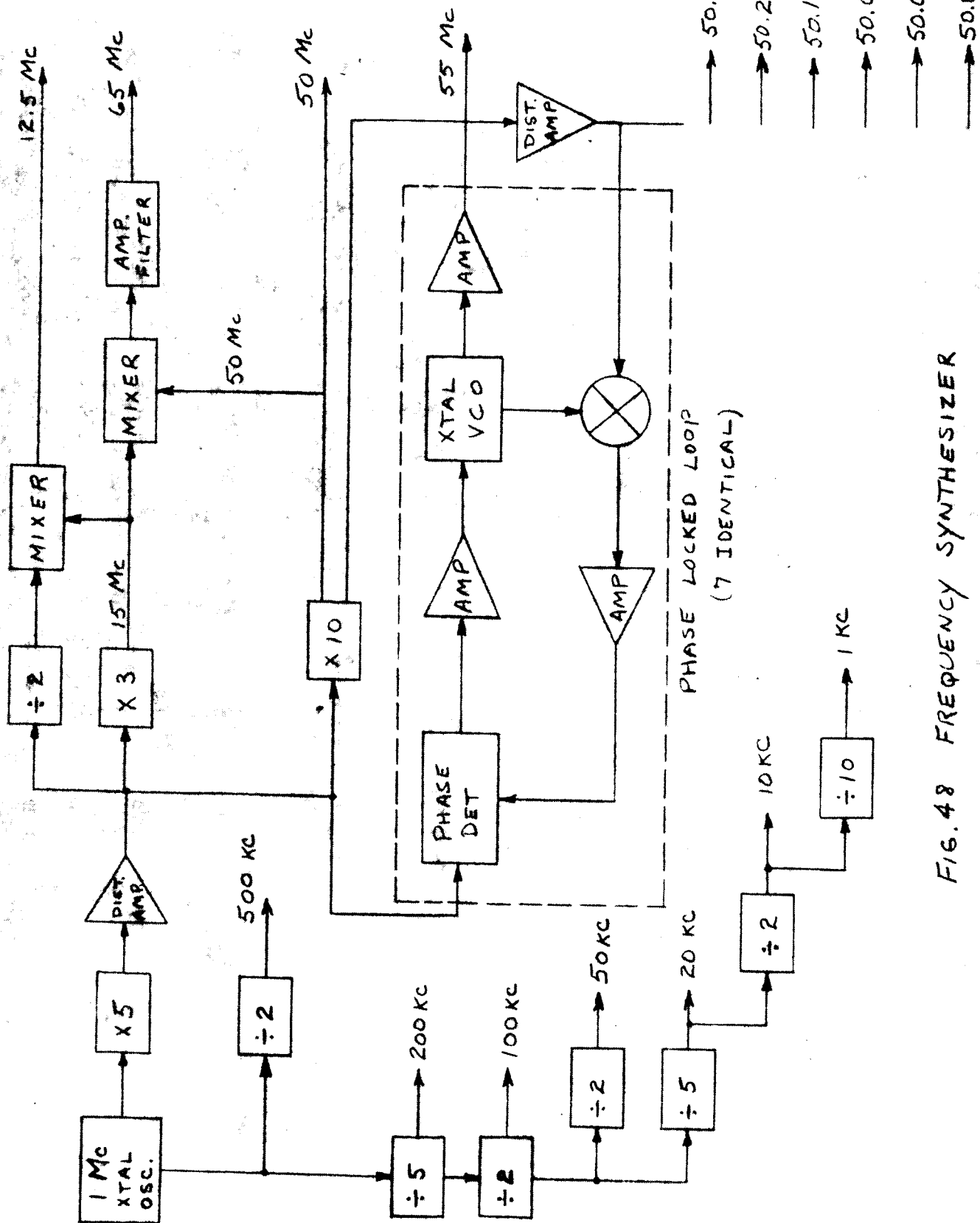


FIG. 48 FREQUENCY SYNTHESIZER



\* The 12.5 mc synthesizer output provides a reference to the P.M. Transmitter. The short term stability of this frequency reference must be compatible with the specified P.M. Receiver carrier tracking loop RMS phase noise error.

F. Test Instrumentation Subsystem

The Test Instrumentation Subsystem is outlined in figure 1. Appendix K includes the details of the Test Plan and Test Instrumentation. A detailed outline of the various makes of the specified test equipment is included plus the recommended choice. Most of the choices are self evident; however, the Spectrum Display unit selection was influenced by relative costs. The Hewlett Packard 851A/855A exhibits superior characteristics; however, its frequency range is far greater than required (10 mc to 400c). Further, its cost is essentially three times the nearest competitor; namely, the Singer Metric SPA-3A. The Singer Metric was chosen on the basis of adequate characteristics and lower price.

Appendix K includes the suggested Test Plan for correlating the specification and hardware performance. Briefly, test systems for measuring the following are included:

1. Short Term Stability
2. Long Term Stability
3. Frequency Response
4. Phase Deviation
5. Incidental A. M.
6. Incidental Angle Modulation
7. Deviation Linearity

8. Percent Modulation
9. Phase Linearity
10. APC Loop Bandwidth
11. AGC Loop Bandwidth
12. Spurious and Carrier Rejection
13. Static Phase Error
14. Filter Impulse Response
15. Frequency Deviation

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G. Linear S/N Summer Noise Power Density Test Results

The S/N Summer Test Results outlined in section II,B of this report are based on average signal power and average noise power measurements. JPL recommended that further tests be made that yield a measure of the noise power density.

1. Introduction

The original scope of work was expanded to include noise power density tests as outlined in table IX.

Center Frequency	Total Noise BW	Increment Spacing	Noise BW Per Increment
50 mc	$\pm 2$ mc	200 kc	50 kc
50 mc	$\pm 100$ kc	20 kc	5 kc
50 mc	$\pm 10$ kc	2 kc	500 cps

Table IX. Specified Noise Power Density Data

Further, the noise power density specification required that the noise power density shall be constant within  $\pm 0.05$  DB over the  $\pm 2$  mc bandwidth as outlined in table IX. A simplified block diagram of the system intended to measure the spectral density is shown in figure 49.

The system of figure 49 is described briefly as follows: The band limited noise (centered on 50 mc) was down converted by the multiplier (phase detector) such that the input noise centered on 50 mc is referenced to DC at the output. The down converted noise was filtered by a 3 pole Butterworth low pass filter to establish the noise bandwidth in accordance with column 4 of table IX. The filtered noise provided the input to the sample and hold circuit which in turn provided the input to the A/D converter.

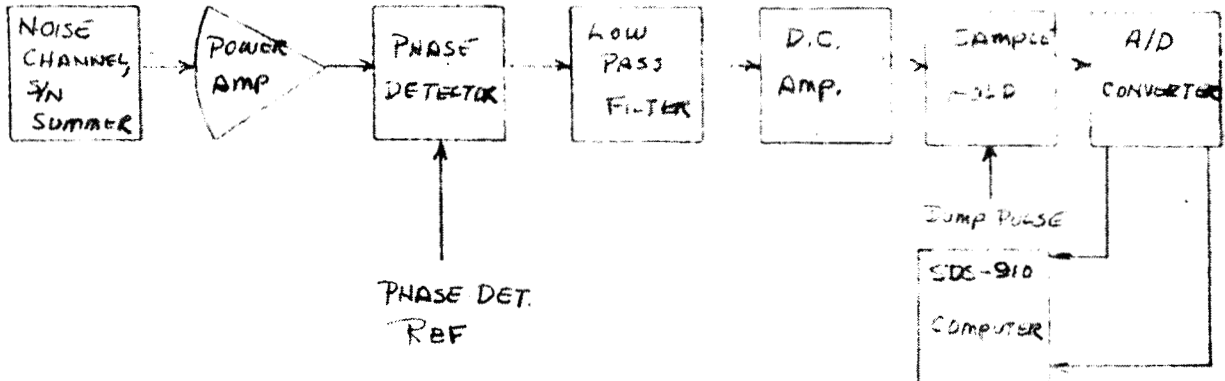


Figure 49. Simplified Diagram of Noise Power Density Test System

The A/D converter converted each sample input to one of 1024 levels (10 bit word) for processing in the SDS-910 computer. The RMS values were computed by squaring the sample values, summing and dividing by the total number of samples and computing the square root. The incremental spacing of the selected noise bandwidth was achieved in accordance with column 3 of table IX by changing the phase detector reference frequency.

## 2. Measurement Techniques

The noise power density was specified as a constant, within  $\pm 0.05$  dB over a  $\pm 2$  mc bandwidth centered at 50 mc. Ideally, the measurement system should be an order of magnitude more accurate than the parameter to be measured. However, the accuracy goal of the noise power test set was established as  $\pm 0.01$  dB ( $\pm 0.1\%$  in voltage), a

compromise between realism and the ideal. The simplified system outlined in figure 49 was inadequate for the following reasons. The computer processes absolute voltage samples of the noise from the noise source; therefore, changes in gain or drift in DC levels of any of the components between the noise source and the A/D converter are manifest as changes in the noise source. The absolute accuracy of the system shown in figure 49 proved inadequate. Therefore, the system was modified to include the details outlined in figure 50.

The operation of the system shown in figure 50 is outlined briefly as follows: Initially, the noise source output was split in a hybrid and a portion of the noise power measured on the Weinschel Dual Channel System. The remaining hybrid noise output was processed as outlined earlier and measured on the SDS-910 computer. Adjacent in time the noise source input to the hybrid was disconnected and a C.W. signal injected at an additional hybrid port at a suitable frequency difference from the phase detector reference. The C.W. signal was also simultaneously measured on the Weinschel Dual channel and the SDS 910 computer. The runs were made in pairs whereby the C.W. data was used to calibrate the system for the noise measurement. The RMS values calculated by the computer were used to establish an equivalent system gain from the hybrid (summing point) to the A/D converter. System gain changes and drifts are common to both the noise measurement and CW reference measurement. Assuming the system drift rate is such that conditions are essentially the same during adjacent time measurement of noise and CW reference, (a valid assumption) the noise power density was computed from the following relationships:

Noise & CW Reference Power  
Measured on Weinschel Dual  
Channel

I DB

RMS Values Measured on  
SDS 910 Computer

M

Preset Reference Level  
(A Computer Constant)

R

Equivalent system noise gain  
from hybrid summing point  
to A/D converter

$G_{DB}$  noise

Equivalent system CW gain  
from hybrid summing point  
to A/D converter

$G_{DB}$  (CW Reference)

The following equations are evident

$$G_{DB}(\text{NOISE}) = 20 \log_{10} \left( \frac{M}{R} \right) - I_{DB} \quad (80)$$

$$G_{DB}(\text{CW REFERENCE}) = 20 \log_{10} \left( \frac{M}{R} \right) - I_{DB} \quad (81)$$

$$\Delta_{DB} = G_{DB}(\text{NOISE}) - G_{DB}(\text{CW}) = 10 \log (2 N_o B) + K \quad (82)$$

$N_o$  = Noise Power Density in the vicinity of the phase detector  
reference

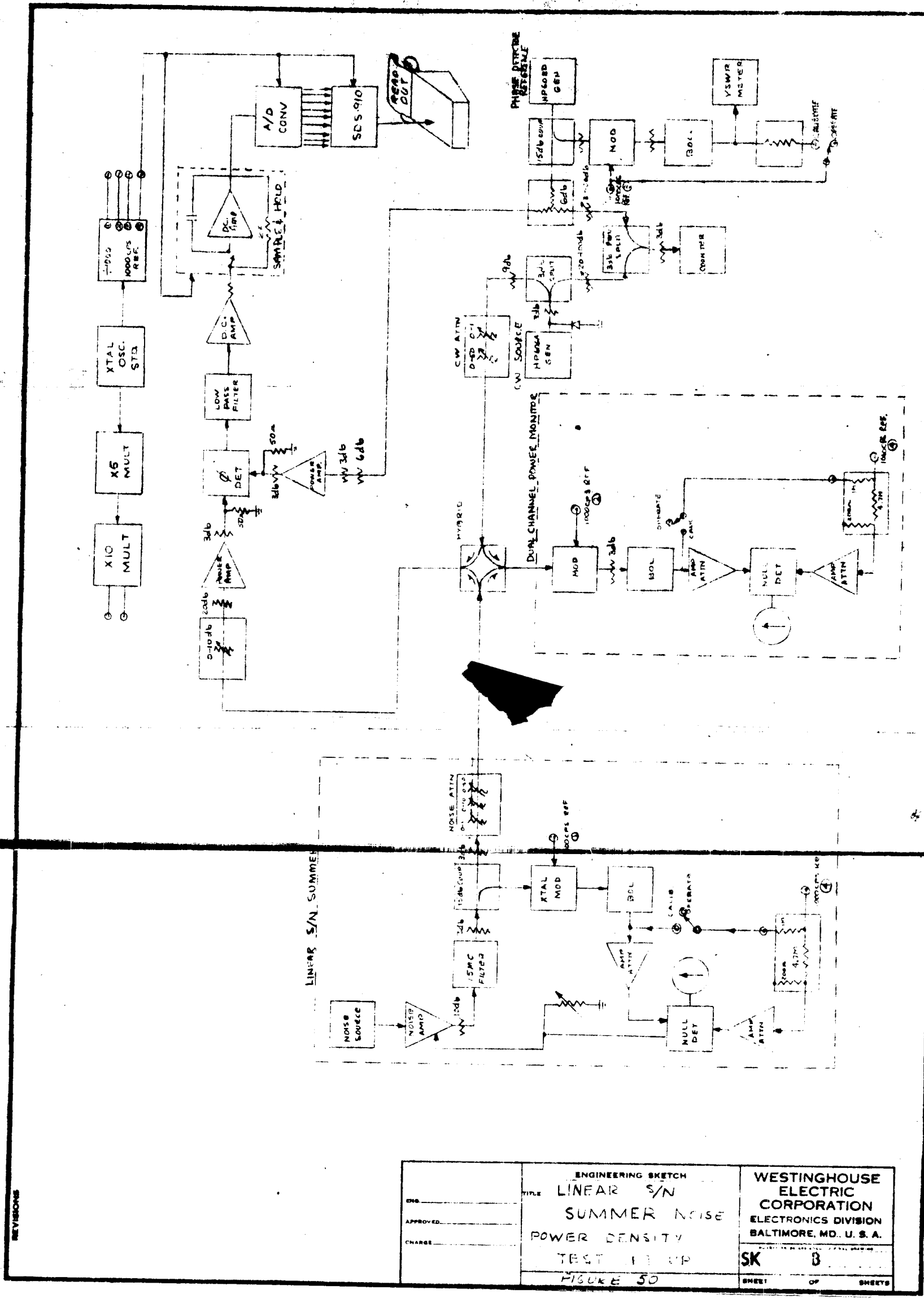
B = Low Pass Filter Bandwidth

K = Correction for differences of attenuation, input level  
and reference levels between noise and CW.

65-325

65-325

65-325



REVISIONS	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION ELECTRONICS DIVISION BALTIMORE, MD. U. S. A.
	TITLE	
	LINEAR S/N	
	SUMMER NOISE	
POWER DENSITY	TEST 11 UP	SK 8
FIGURE 50	SHEET 1 OF 1 SHEETS	

### 3. Conclusions

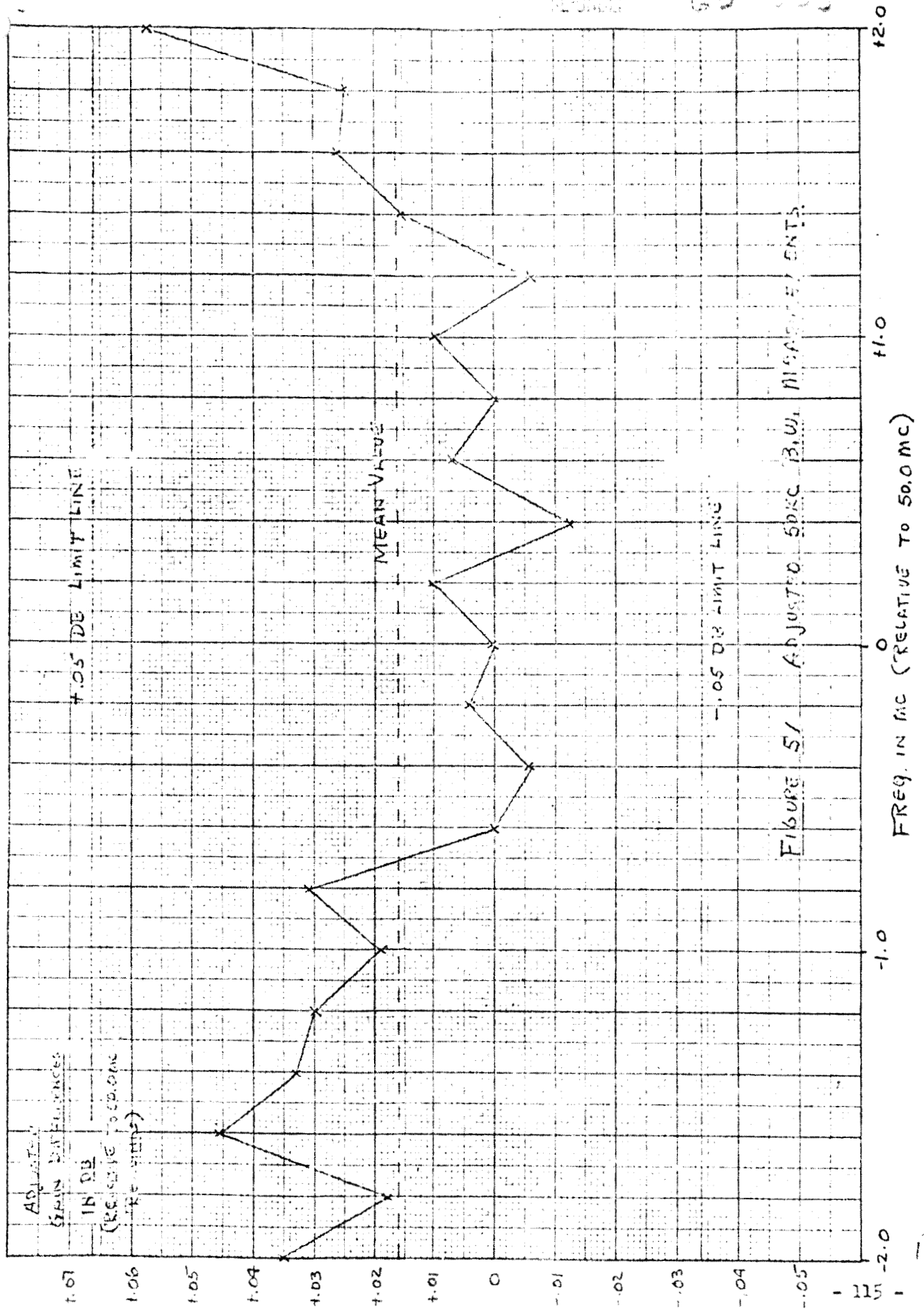
Figure 51 indicates the test results of the noise power measurements of 50 KC noise bandwidth taken over a reference frequency range of  $50.0 \pm 2$  mc in steps of 200 KC. The plot is adjusted to cancel the frequency response slope attributed to the noise amplifier, noise filter combination. The latter was measured at nominal noise amplifier AGC voltage to an accuracy of  $\pm 0.01$  DB with the Weinschel Dual Channel System. It was decided to measure the noise power deviations from this curve rather than retune the noise amplifier or noise filter. The noise measurements from 50.0 mc to 48.0 mc were taken in descending order of frequency over a 5 day period. No unusual results were noticed until the phase detector reference frequency was retuned to 50.2 mc to take measurements with ascending frequency. It was suspected that this result was too low. This was confirmed by repeating the 50.0 mc measurements which yielded 2 groups close together but .03 DB lower than the original readings. The 50.0 mc measurement was retaken the next day and found to be 0.65 DB below the original pair taken a week earlier. The drift in the 50 mc reading was thereby confirmed and must be taken as evidence that some uncontrolled variable was causing significant changes in the measuring equipment or the noise power density at the summer terminals. It was decided not to stop the tests to search for the cause of the variation as past experience has shown that this could consume a great deal of time. The other sets of measurements consisted of 11 points instead of 21; therefore, it was felt that a set could be completed in 2 days and repetition of one point would serve to tie the results together. Therefore, the 50 KC noise bandwidth results are shown in figure 51 with the results adjusted for agreement at the 50.0 mc point and corrected for the frequency response of the noise amplifier noise filter. As shown all points lie within the range of  $\pm 0.05$  DB.



13  
Figure 52 indicates the test results of the noise power measurements of 5 KC noise bandwidth over the frequency range  $50.0 \pm 0.10$  mc in 20 KC steps. A total of 18 groups of measurements was made in a period of 3 days. The measurement at 50.04 mc was taken 3 times, once each day, however no significant drift was evident. Therefore, the mean noise/CW gain differences  $\bar{\Delta}$  are plotted in figure 52 without adjustment.

The overall mean is 13.602 DB and limit lines of  $\pm .05$  DB about the mean as shown in figure 52, allowing a tilt of +0.010 DB from 49.90 mc to 50.01 mc for the noise amplifier frequency response. All measured points are within the  $\pm 0.05$  DB limit.

Figure 53 indicates the test results of the noise power measurements of 500 cps noise bandwidth taken over a reference frequency range of  $50.0 \pm 10$  KC in 2 KC steps. The first day, steps were taken from 50.0 mc down to 49.990 mc. The second day the range from 50.002 mc to 50.010 mc was covered and 49.998 mc repeated. A difference of 0.07 DB between the means for the two days was observed which is almost four times the pooled standard deviation and definitely indicated drift. The drift was attributed to the increased drive level to the phase detector required to maintain a suitable noise voltage from the 500 cps bandwidth noise filter. Further, 50 mc leakage from the phase detector reference source was suspect as a contributor to drift. The latter drift source was cancelled between readings. On a third day four points were taken across the 20 KC range. These measurements were taken at reduced noise input level for greater gain stability. The results indicated small differences between points. The data of figure 53 shows the earlier sets adjusted to agree at 49.998 mc with the four later points superimposed to give the same mean value. There is no appreciable tilt for the noise amplifier/filter frequency response over this range. As shown all points are within the  $\pm 0.05$  DB limit lines.



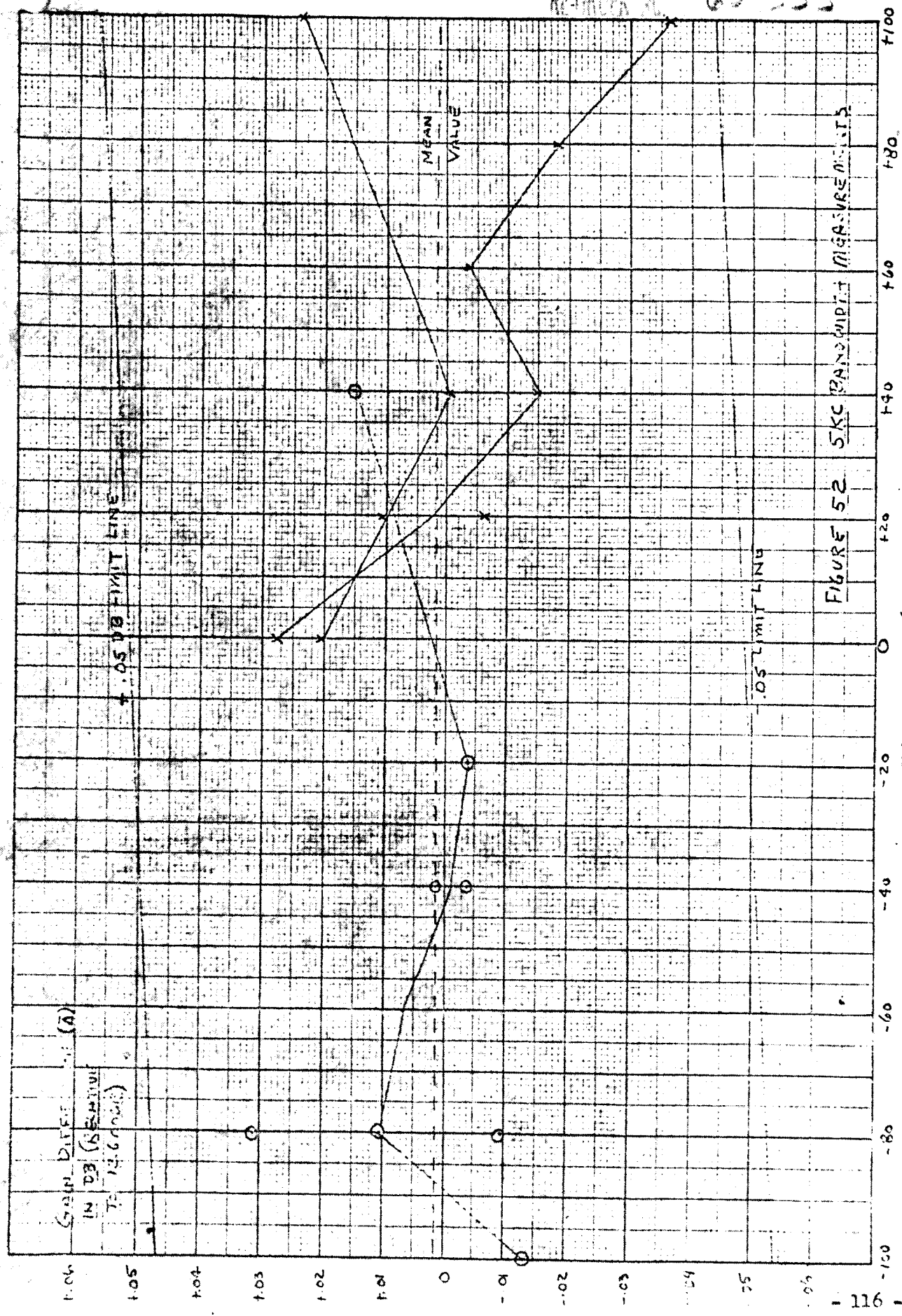
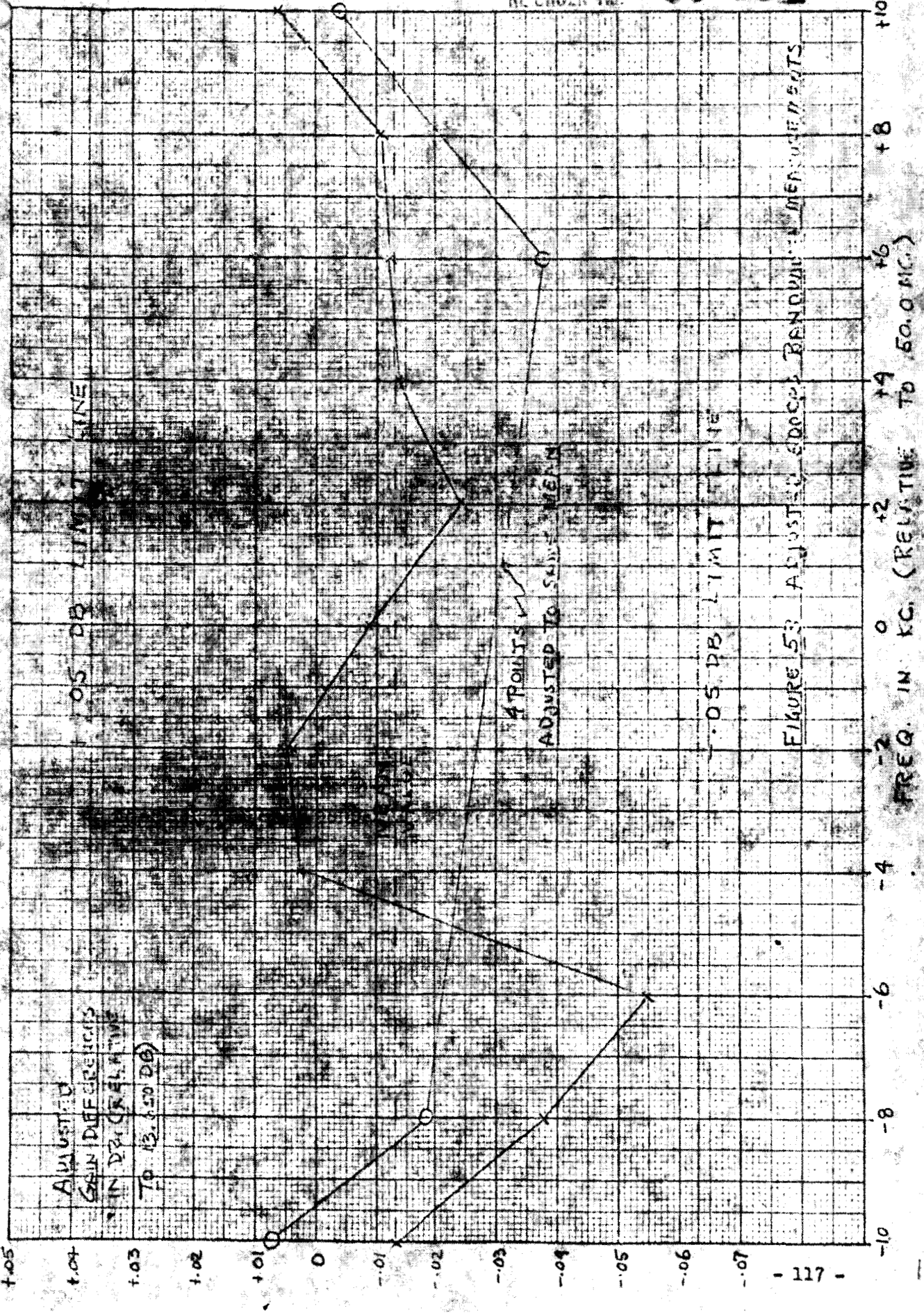


FIGURE 52 5KC BANDWIDTH MEASUREMENTS

FREQ IN KC (RELATIVE TO 50.0 MC)



#### H. MECHANICAL PLAN R-F TEST CONSOLE

The R-F Test Console will be packaged in four 19 inch cabinet racks, located side by side. The proposed arrangement is shown in figure 54.

The cabinets will have welded corners and the seams and openings will be suitably gasketed and shielded to provide maximum r.f.i. attenuation consistent with the state-of-the-art and the limitations imposed by the commercial units forming a part of the assembly. Doors will be provided on the rear for access to the interior and on the front to further aid in the r.f.i. attenuation. A retractable work surface and a utility drawer will be provided in the transmitter cabinet. The work surface will be at desk height. The equipment will be painted in a manner to be defined by the cognizant JPL engineer.

Modular construction will be used in the self-manufactured chassis such as the transmitter and receivers. The packaging concept is illustrated in figures 55 and 56. Each circuit module will be composed of an 8" x 4" aluminum plate on which a Micarta board is mounted. The Micarta board will carry the circuit components and a connector. The component layout will be similar to a printed circuit board, however, point-to-point interconnecting wiring will be used. The aluminum plate will provide an r-f shield for the circuit when the modules are inserted into a rack in a card file arrangement. It is proposed to assemble the boards in a double row arrangement in a slide-out drawer.

RMS VOLT-METER	POWER METER	COUNTER	BOLOMETER PREAMPLIFIER	WEINSCHEL ATTENUATOR
DIGITAL VOLT-METER		OSCILLOSCOPE	DIFFERENTIAL NULL DETECTOR	PHASE SHIFTERS
PHASE NOISE INSTRUMENTATION			POWER SAMPLER	F M RECEIVER
SPECIAL TEST INSTRUMENTATION		SPECTRUM ANALYZER DISPLAY	ATTENUATION CALIBRATOR	P M RECEIVER
FREQUENCY SYNTHESIZER			LEVEL CONTROL	P M RECEIVER
F M/P M TRANSMITTER		SPECTRUM ANALYZER	PRECISION STEP ATTENUATOR	PHASE DETECTOR
RETRACTABLE WORK SURFACE		FUNCTION GENERATOR	PRECISION STEP ATTENUATOR	PHASE DETECTOR
UTILITY DRAWER		OSCILLATOR	NOISE GENERATOR	POWER DISTRIBUTION PANEL
POWER DISTRIBUTION PANEL & POWER SUPPLIES		BLANK PANEL	NOISE AMPLIFIER	POWER SUPPLY
BLOWER		BLOWER		POWER SUPPLY
				POWER SUPPLIES
				BLANK PANEL
				BLOWER

TRANSMITTER RACK COMMERCIAL INSTR. LINEAR S/N SUMMER RECEIVER RACK  
R-F TEST CONSOLE CABINETS FIGURE 54

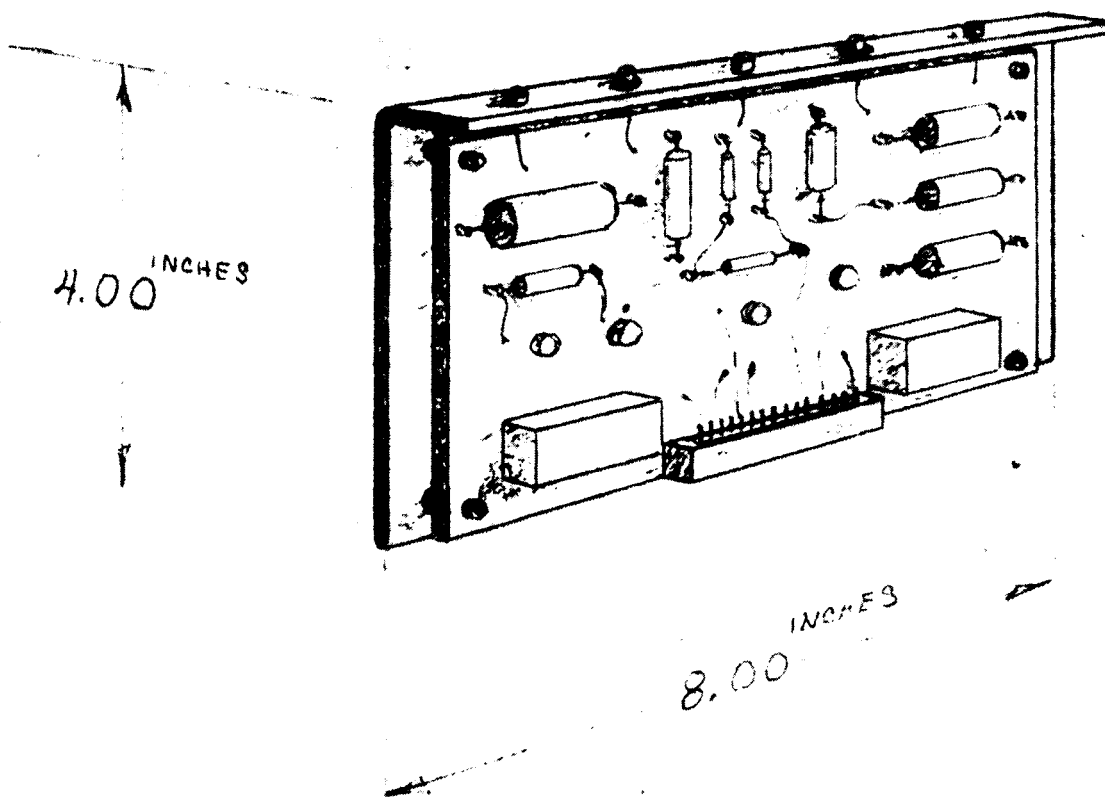
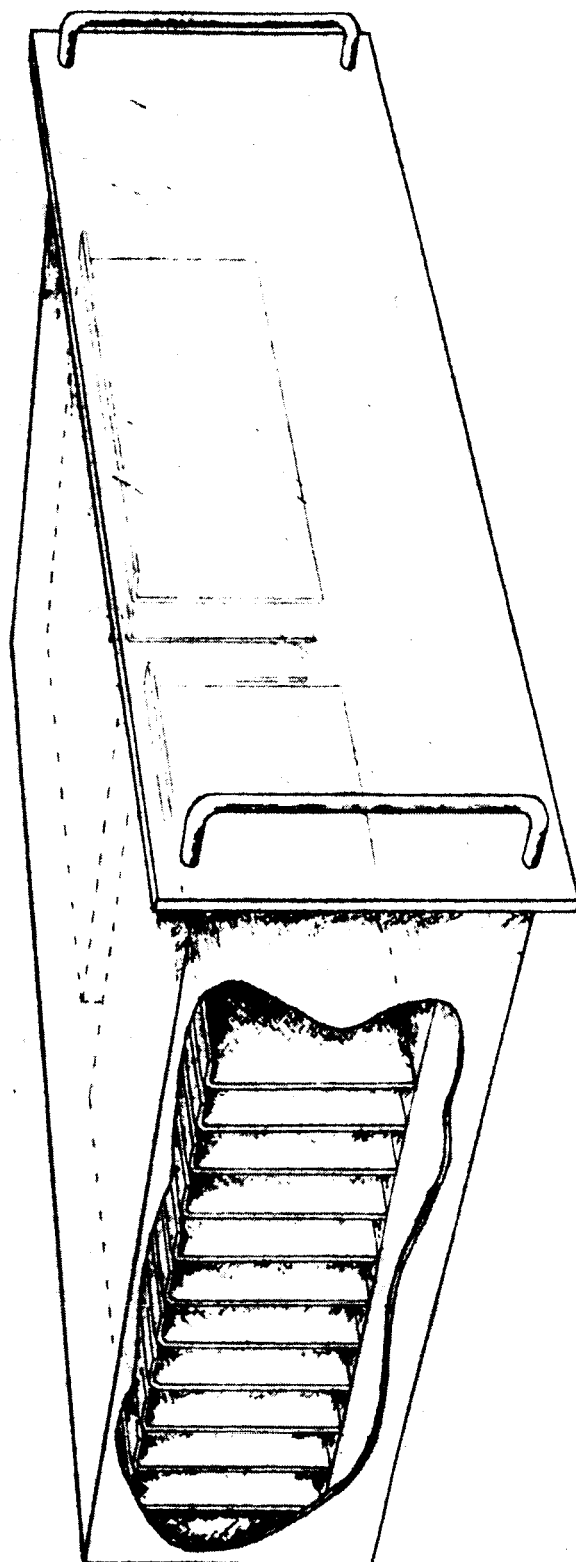


FIGURE 56





Each board will be plugged-into the drawer the same as a printed circuit board. Each plate will have a flange at the top, containing the test points and coaxial connectors.

The following list identifies the modularized chassis and indicates the quantity of modules. In addition to the modules, other required components and sub-assemblies (such as a phase detector in the receivers) will be mounted within the chassis.

1. Synthesizer	21 modules
2. Phase Noise Instrumentation	5 "
3. FM/PM Transmitter	10 "
4. PM Receiver	36 "
5. FM Receiver	13 "

A gasketed cover plate will be used on both the top and the bottom of each drawer to provide r.f.i. sealing. External coaxial connectors and controls will be brought out to the front panel of the drawer. All other external wiring will terminate in a connector at the rear of the drawer, which will mate with a connector of the cabinet wiring. A cable retractor will be used with each drawer to prevent tangling or kinking the cable when opening or closing the drawer.

A vertical cable trough, such as "Panduit" or "Panel Channel" will be provided in each cabinet to carry the intra-cabinet wiring. Inter-cabinet and external wiring will be carried in conduit at the top of the cabinets.

Cooling air will be provided by blowers located at the bottom of the cabinets. The air intake will be at the bottom of the front